CHIRP TRANSFER FUNCTION ANALYZER - RF PROGRAMMABLE CHIRP SYNTHESIZER

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By

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EE-1981-M-CHO-CHI

TO

MY PARENTS

CERTIFICATE

Certified that this thesis, entitled "Chirp Transfer Function Analyzer - RF Programmable Chirp Synthesizer" is a record of the work carried out by Mr. B. Prabhakara Chowdary under my supervision and that this has not been submitted elsewhere for a degree.

Jul. 27,1981

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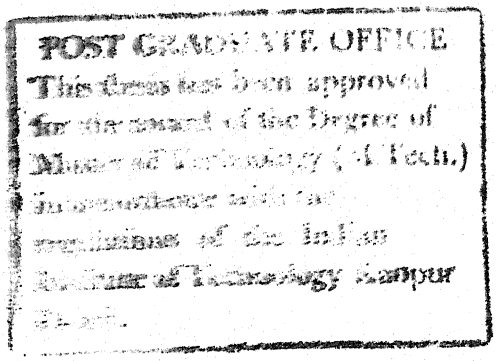

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ABSTRACT

Transfer function analyzer using a chirp signal as an excitation function has many advantages compared to the conventional methods of sinusoidal or pulse testing. The system architecture is discussed in this thesis. The hardware implementation of such system has two components; i)generation of an excitation signal and the local oscillator signal for demodulation ii) the signal processing in the receiver to obtain the transfer function. The signal processing in the receiver to obtain the transfer function is discussed in a companion thesis, " Chirp transfer function analyzer - signal processor". This thesis covers the design and implementation of RF Programmable chirp synthesizer which generates chirp signal as well as its, Carrier frequency simultaneously. The chirp signal parameters vij i) chirp width (Δf), ii) chirp rate (α), iii) chirp sweep time are programmable. It is observed from the experiments that the chirp spectrum becomes flatter and flatter as the time bandwidth product ($T\Delta f$) : increases.

CAMAC Standards are followed for the hardware implementation.

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CHAPTER I

INTRODUCTION

Time invariant linear systems are characterized either by their system function H(w) or impulse response h(t). H(w) and h(t) form a Fourier transform pair.

The system function of a linear system can be evaluated by the following conventional methods 1) Continuous wave excitation method 2) Impulse response method. In the continuous wave excitation method a pure sine wave of a fixed frequency is applied to the linear system and the output H(w) is noted after it reaches a steady state. This procedure is repeated by changing the excitation frequency in steps of $\triangle$ f to cover the entire bandwidth of the linear system. Now the plot of w vs H(w) gives the system function. A disadvantage of this method is that in order to obtain a high resolution spectrum one must keep the frequency increments ($\triangle$f) very small and as a result the measurement consumes a great deal of time. In the impulse response method, an impulse is applied to the linear system and Fourier transform of its time response is found to obtain the system function. A serious disadvantage with this method is that generating an impulse with infinitesimally small width is impracticable. So a pulse of a finite

width is used instead of an impulse. If the system function of a linear system having a bandwidth B Hz is to be found out then the pulse width should be as low as $\frac{1}{2B}$ sec. For broad band systems i.e. systems having very large B, a pulse of very small width must be applied. A disadvantage with the pulse excitation is that it requires large peak power which may saturate the system under study.

The impulse response of a linear system can also be measured by the correlation method (Ref. 1). The scheme is shown in Fig. 1.1.

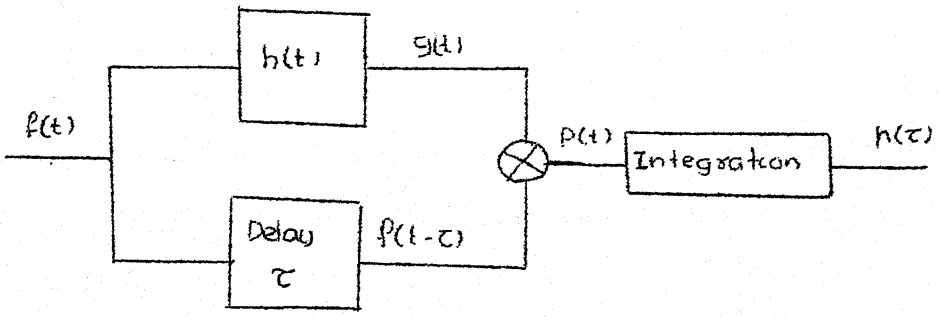


Fig. 1.1: Correlation Method

In Fig. 1.1, f(t) is the excitation to the linear system whose impulse response is h(t) resulting in a response g(t). The excitation function f(t) is delayed by τ and multiplied with g(t) to get p(t).

$$p(t) = g(t) \cdot f(t-\tau)$$

$$= \int_{-\infty}^{\infty} h(x)\, f(t-x)\, dx \cdot f(t-\tau)$$

Now, if we integrate p(t) over the limits $-\infty$ to ∞ we get

$$\int_{-\infty}^{\infty} p(t)dt = \int_{-\infty}^{\infty}\left[\int_{-\infty}^{\infty} h(x)f(t-x)dx\right] f(t-\tau)\, dt$$

$$= \int_{-\infty}^{\infty} h(x)dx \int_{-\infty}^{\infty} f(t-x).f(t-\tau)\, dt \qquad (1.1)$$

The term in square brackets in the above equation is nothing but the auto-correlation of excitation function, f(t).(Ref.2) If we choose f(t) such that its autocorrelation is an impulse function, $u_o(\tau - x)$, then the integrater output leads to

$$h(\tau) = \int_{-\infty}^{\infty} h(x)\ u_o(\tau - x)\, dx \qquad (1.2)$$

Now by varying the delay τ one can get the impulse response at other points. Two commonly used signals having impulsive autocorrelation function are

1) Pseuedo Random Binary Sequence (PRBS)

2) Chirp Signal

The former one is digital signal having only two states and the latter is analog. In this thesis the chirp signal is being used as excitation for system function evaluation. The chirp signal has the advantages of having larger average power when compared to pulse excitation and uniform power spectral density over its specified bandwidth. In the

correlation method shown in Fig. 1.1, the impulse response samples are Fourier transformed to obtain system function. Thus the scheme in general is a two step process. However with the chirp signal as excitation with a modification in the signal processing we can obtain the system function directly. This is discussed in detail in Chapter II.

Applications:

Since a great majority of engineering systems are modelled as time invariant linear systems, there are innumerable situations requiring the knowledge of the system function and one can measure it using one of the three methods discussed above. The choice of the method is dictated by the ease of using one method over other methods.

For example, the phenomena of Nuclear Magnetic Reasonance presents in most isotopes of the elements closely approximate to a time independent linear system "System Function" under non-saturating conditions. System function of this linear system though can be obtained using any of the above methods, the chirp technique offers some advantages interms of instrumentation as well as accuracy. (Ref. 3)

This thesis entitled "Chirp-transfer function analyzer-RF programmable chirp synthesizer" is a companion thesis to the work done by S.M. Rao towards his M.Tech. thesis, entitled

"Chirp transfer function analyzer- Signal Processor". Both the systems put together become a complete "Chirp-transfer function analyzer". The system has been developed for a set of specifications keeping in mind its possible use in NMR spectroscopy.

In Chapter II the theory behind the operation of "Chirp-transfer function analyzer" has been described. Analysis of the chirp signal is also given.

In Chapter III, a brief review of frequency synthesis techniques in particular coherent indirect synthesis scheme using digital phase locked loop, has been discussed. In Chapter IV the design and fabrication of RF programmable chirp synthesizer has been dealt with using the phase locked loop frequency synthesis technique described in Chapter III. Experiments and results are given in Chapter V and conclusions and recommendations for further work are given in Chapter VI.

CHAPTER II

CHIRP TRANSFER FUNCTION ANALYZER

Before we go into the analysis of the chirp transfer function analyzer a brief discussion on the low pass equivalent of band pass system and the properties of the chirp signal are in order.

2.1 Low pass equivalence of a Band pass System:

A band pass signal f(t) can be written as;

$$f(t) = f_c(t) \cos w_c t - f_s(t) \sin w_c t \qquad (2.1)$$

It can also be equivalently described in terms of the complex envelope as

$$f(t) = \mathrm{Re}\left\{ \tilde{f}(t)\, e^{jw_c t} \right\} \text{ where } \tilde{f}(t) = f_c(t) + j\, f_s(t)$$

The low pass signals $f_c(t)$ and $f_s(t)$ are known as the inphase and quadrature components.

The impulse response of a band pass system can similarly be described in terms of its inphase and quadrature components as;

$$\tilde{f}(t) = h_c(t) \cos w_c t - h_s(t) \sin w_c t$$

$$= \mathrm{Re}\left\{ \tilde{h}(t)\, e^{jw_c t} \right\} \qquad (2.2)$$

when the band pass signal f(t) is fed to the band pass system with the impulse response h(t), the output g(t) is given by the convolution of f(t) with h(t) as;

$$g(t) = \int_{-\infty}^{\infty} h(x)\ f(t-x)\ dx \qquad (2.3)$$

Substituting the equivalent low pass representations for f(t) and h(t) it can be shown that the output g(t) can be written as

$$g(t) = g_c(t)\cos w_c t = g_s(t)\sin w_c t$$

$$= \mathrm{Re}\left\{\tilde{g}(t)\ e^{jw_c t}\right\} \qquad (2.4)$$

where

$$g_c(t) = \frac{1}{2}\ \mathrm{Re}\left[\tilde{h}(t)\ \textcircled{x}\ \tilde{f}(t)\right]$$

and $$g_s(t) = \frac{1}{2}\ \mathrm{Im}\left[\tilde{h}(t)\ \textcircled{x}\ \tilde{f}(t)\right] \qquad (2.5)$$

Thus the band pass system can be conveniently studied using the equivalent low pass systems as depicted in Fig. 2.1

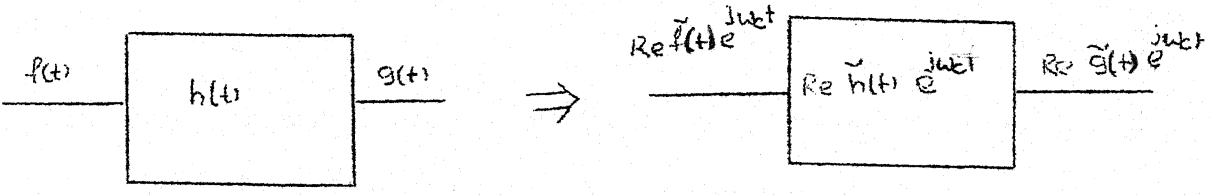


Fig. 2.1(a) Band pass system

Fig. 2.1(b) Complex representation.

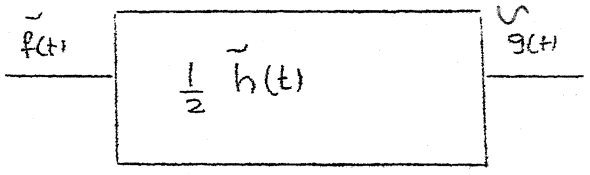


Fig. 2.1(c) equivalent low pass representation

2.2 Chirp Signal:

The chirp signal also known as the linear FM signal, is a frequency modulated wave whose instantaneous frequency varies linearly with time and thus $s(t)= \cos(w_c t+ \alpha t^2)$. The complex envelope $z(t)$ of the chirp signal is given by $z(t) = e^{j\alpha t^2}$. We will now derive the spectrum of the chirp signal of infinite duration as well as of finite duration.

Case 1: Chirp signal extending from $-\infty$ to $+\infty$;

The chirp signal can be represented as; (Ref.4)

$$z(t) = e^{j\alpha t^2} \quad -\infty \text{ to } +\infty \tag{2.7}$$

$$z(w) = \text{F.T. of } z(t) = \int e^{j(\alpha t^2 - wt)}\, dt \tag{2.8}$$

since $\alpha t^2 - wt = \alpha(t - w/2\alpha)^2 - \frac{w^2}{4\alpha}$

If we put $\sqrt{\alpha}t - \frac{w}{2\sqrt{\alpha}} = y$, we have

$$y^2 = \alpha t^2 + \frac{w^2}{4\alpha} - wt \quad \text{and} \quad dt = \frac{dy}{\sqrt{\alpha}}$$

or,

$$\alpha t^2 - wt = y^2 - \frac{w^2}{4\alpha} \tag{2.9}$$

Substituting equation (2.9) in equation (2.8) we get;

$$z(w) = \frac{1}{\sqrt{\alpha}} e^{-jw^2/4\alpha} \int_{-\infty}^{\infty} e^{jy^2} dy$$

$$= \frac{2}{\sqrt{\alpha}} e^{-jw^2/4\alpha} \int_{0}^{\infty} e^{jy^2} dy$$

$$= \sqrt{\frac{\pi}{\alpha}} e^{j\pi/4} e^{-jw^2/4\alpha} \tag{2.10}$$

Power spectral density of $z(w) = |z(w)|^2 = \left| \sqrt{\frac{\pi}{\alpha}} e^{j\pi/4} e^{-jw^2/4\alpha} \right|^2$

$$|z(w)|^2 = \pi/\alpha \tag{2.11}$$

Equation (2.11) shows that the power spectral density of chirp signal which extends from $-\infty$ to $+\infty$ depends only on α, the time rate of change of frequency.

Case 2: Chirp signal is time limited, $-T/2 < t < T/2$ (Ref. 2)

The spectrum of linear FM in this case can be found as

$$s(w) = \int_{-T/2}^{T/2} \cos\left[w_o t + \frac{\alpha t^2}{2}\right] \exp(-jwt) dt \tag{2.12}$$

$$= \frac{1}{2} \int_{-T/2}^{T/2} \exp\left[j \left\{ (w_o - w)t + \frac{\alpha t^2}{2} \right\} \right] dt +$$

$$\frac{1}{2} \int_{-T/2}^{T/2} \exp\left[- j \left\{ (w_o + w)t + \frac{\alpha t^2}{2} \right\} \right] dt \qquad (2.13)$$

The second integral defines the spectrum at negative frequencies and has a negligible contribution at positive frequencies if the ratio of centre frequency to bandwidth is large. The essential assumption here is that the tail of the negative frequency spectrum has an infinitesimally small value in the region of the positive spectrum. This is a realistic assumption for the ratio of $w_o/\Delta w$ sufficiently large. By simplifying the square of the bracketed term in equation (2.13) as in case (1) and eliminating the second term z(w) is expressed as;

$$s(w) = \frac{1}{2} \exp\left[-j \left(\frac{(w - w_o)^2}{2\alpha} \right) \right] \int_{-T/2}^{T/2} \exp\left[j \pi/2\alpha \left(t - \frac{w - w_o}{\alpha} \right)^2 \right] dt \qquad (2.14)$$

The variable in equation (2.14) can be changed by letting;

$$\sqrt{\alpha}\left(t - \frac{w - w_o}{\alpha} \right) = \sqrt{\pi} x \quad \text{so that} \quad dt = \sqrt{\pi/\alpha}\, dx$$

and the spectrum becomes:

$$s(w) = \frac{1}{2}\sqrt{\pi/\alpha}\exp\left[-j\left\{\frac{(w-w_o)^2}{2\alpha}\right\}\right]\int_{-X_1}^{X_2}\exp\left[j\frac{\pi x^2}{2}\right]dx$$

where

$$X_1 = \frac{\alpha T/2 + (w-w_o)}{\sqrt{\pi\alpha}}, \quad X_2 = \frac{\alpha T/2 - (w-w_o)}{\sqrt{\pi\alpha}}$$

This yields;

$$s(w) = \frac{1}{2}\sqrt{\pi/\alpha}\exp\left[-j\left\{\frac{(w-w_o)^2}{2\alpha}\right\}\right]\left[C(X_1)+j\,D(X_1) + C(X_2) + j\,D(X_2)\right] \qquad (2.15)$$

where

$$C(X) = \int_0^X \cos\frac{\pi y^2}{2}\,dy \text{ and } D(X) = \int_0^X \sin\frac{\pi y^2}{2}\,dy$$

are the Fresnel integrals, which have the property $C(-X) = -C(X)$ and $D(-X) = -D(X)$. It is helpful to consider the linear FM spectrum as having three major components as below

1) Amblitude term:

$$|s(w)| = \frac{1}{2}\sqrt{\pi/\alpha}\left\{\left[C(X_1)+C(X_2)\right]^2 + \left[D(X_1)+D(X_2)\right]^2\right\}^{1/2}$$

For large values αT^2, the spectrum is flat and limited to a bandwidth of $2\alpha T$.

2) Square law phase term:

$$\phi_1(w) = \frac{(w-w_o)^2}{2\alpha}$$

3) Residual phase term:

$$\phi_2(w) = -\tan^{-1}\left[\frac{D(X_1)+D(X_2)}{C(X_1)+C(X_2)}\right]$$

For large values of T Δf the ratio $\frac{D(X_1)+D(X_2)}{C(X_1)+C(X_2)} = 1$

hence $\phi(w)$ approximates to a constant phase angle $\pi/4$. Fig. 2.2 plots $|s(w)|$ and $\phi(w)$ for three different values of $2\alpha T^2$, a measure of the time bandwidth product. It can be observed from the Fig. 2.2, if the time band-width product is made large, the finite duration chirp signal very closely approximates the infinite duration chirp signal.

2.3 Chirp transfer Function Analyzer: Ref. 5

The analysis of the chirp transfer function analyzer is carried out in the form of the low pass equivalent system. The schematic of the analyzer is shown in Fig. 2.3. The response $\tilde{g}(t)$ can be derived as follows.

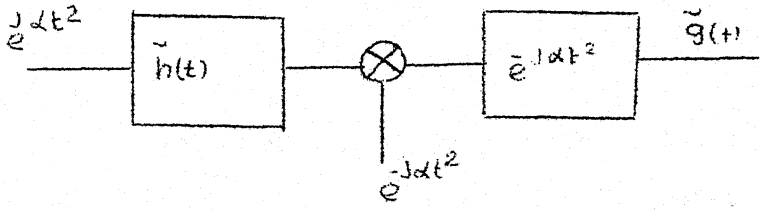
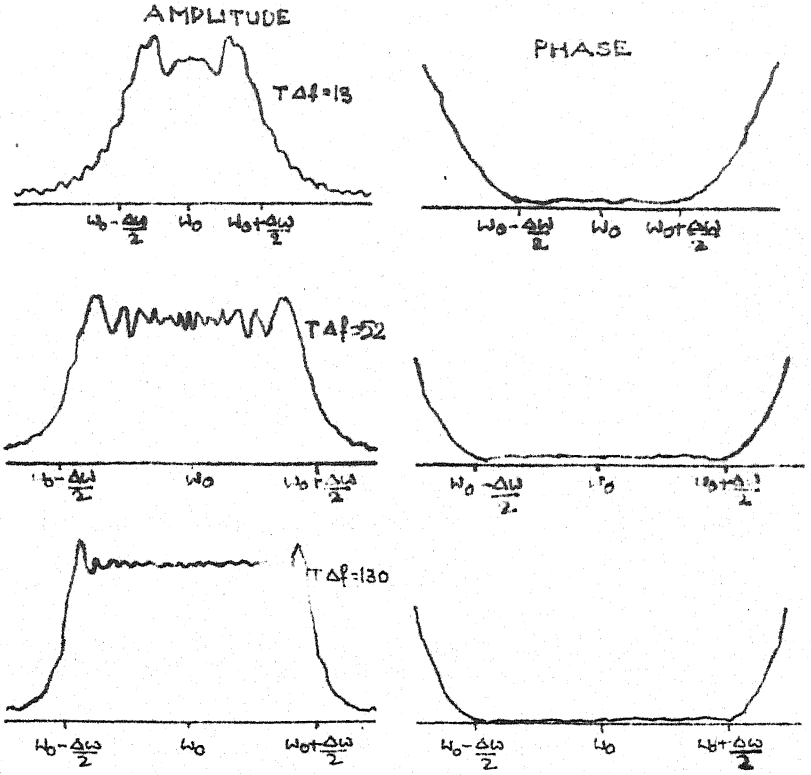


Fig. 2.3: Chirp transfer function analyzer.



G 2.2 Linear FM Spectra after removal of square law phase term

$$\tilde{g}(t) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} \tilde{h}(x)\, e^{j\alpha(\tau-x)^2}\, e^{-j\alpha t^2}\, e^{j\alpha(t-\tau)^2}\, dx \cdot d\tau$$

$$= \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} \tilde{h}(x)\, e^{j\alpha\left[(\tau-x)^2 - \tau^2 + (t-\tau)^2\right]}\, dx \cdot d\tau$$

$$= \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} \tilde{h}(x)\, e^{j\alpha\left[\tau^2+x^2-2\tau x - \tau^2 + t^2 + \tau^2 - 2t\tau\right]} dx \cdot d\tau$$

$$= \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} \tilde{h}(x)\, e^{j\alpha\left[\tau-(t+x)\right]^2} e^{-j2\alpha tx}\, dx \cdot d\tau$$

$$= \int_{-\infty}^{\infty} \tilde{h}(x)\, e^{-j2\alpha tx}\left[\int_{-\infty}^{\infty} e^{j\alpha\left[\tau-(t+x)\right]^2} d\tau\right] \cdot dx$$

$$= \sqrt{\pi/\alpha}\; e^{j\pi/4} \int_{-\infty}^{\infty} \tilde{h}(x)\, e^{-j2\alpha tx}\, dx$$

$$\tilde{g}(t) = \sqrt{\pi/\alpha}\; e^{j\pi/4}\; \tilde{H}(2\alpha t)$$

It shows that the response $\tilde{g}(t)$ will give the system function.

2.4 Implementation:

The schematic of the implementation of the chirp transfer function analyzer for band pass systems is shown in Fig. 2.4 (Ref. 5).

The chirp signal $\cos(w_c t + \alpha t^2)$, and the reference signals $2 \cos w_c t$, $2 \sin w_c t$ are generated by the programmable chirp synthesizer. Coherent detector processes further processed by the power spectral density evaluation module (PSDE), shown with dotted lines in Fig. 2.4, to give $(H(2\alpha t))^2$.

For a low pass system, the coherent detectors are not required and the output of the linear low pass system is directly connected to the Real input of the PSDE and Imaginary input is grounded.

In the next chapter a brief survey of methods of frequency synthesis is discussed for the design of programmable chirp frequency synthesizer.

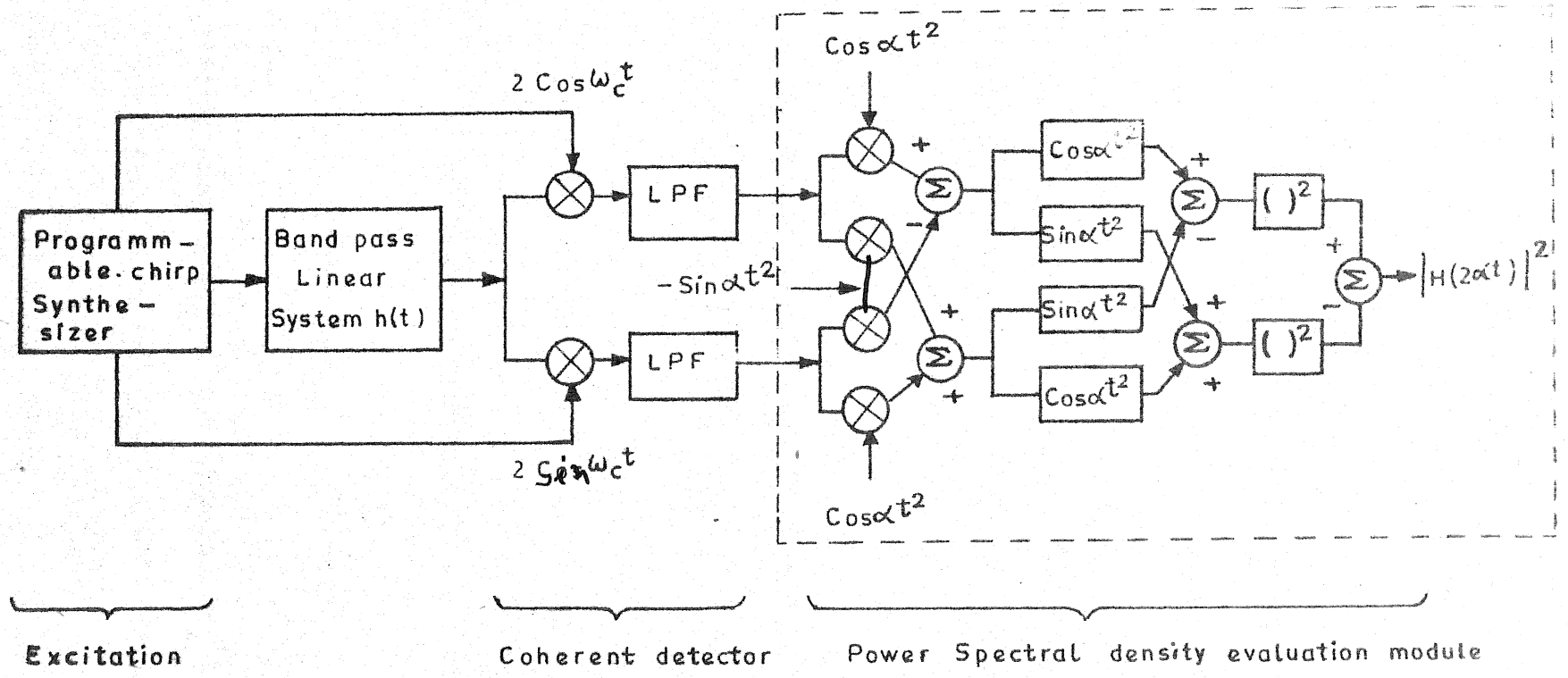


FIG.2.4 Implementation of chirp transfer function analyzer.

CHAPTER III

PROGRAMMABLE FREQUENCY SYNTHESIZERS

In this chapter a survey of the techniques of frequency synthesis widely used in the realization of frequency synthesizers with diverse performance specifications is made and examined. The theory of phase locked loops fundamental to the coherent indirect scheme of frequency synthesis which is most popular today is built up for use in the design of the frequency synthesizers for the present application of chirp transfer function analyzer.

3.1 Frequency Synthesizers:

The technology related to the transfer of the salient features of a standard frequency source to any other predetermined range of frequencies is called frequency synthesis and is accomplished on a general purpose basis by instruments called frequency synthesizers. Frequency range, frequency resolution, programmability, switching time, spurious signals and noise, long term stability and short term stability are the parameters of major importance in characterizing a frequency synthesizer. These parameters are defined and elaborated in the following section.

3.1.1 Frequency synthesizer properties: [Ref. 6]

The frequency synthesizer is a relatively complicated

system involving many components, and usually a number of properties must be specified to characterize its performance. The required performance specifications of these parameters depend upon the application of the synthesizer.

1) Frequency range:

The range of frequencies made available by a frequency synthesizer may vary from a narrow band to broad band in the frequency spectrum ranging from D.C. to microwave. Over these frequency range the number of discrete frequencies may vary from as few as 100 to as high as 5×10^9.

2) Frequency resolution:

Resolution is the minimum frequency difference between any two adjacent output frequencies. Synthesizers usually generate all frequencies within a specified output band with identical spacing as there is little economic advantage to delete some frequencies or to provide non-uniform spacing. The desired resolution depends largely on the application and may be as crude as 100 KHz or as fine as 0.001 Hz or better.

3) Programmability:

Most of today's frequency synthesizers provide for digital programming of the output frequencies. This renders computer control of the synthesizer.

4) Switching time:

Switching is the time between a command to switch to a different frequency and the time output frequency settles down to the new frequency. Switching time, some times, becomes an important parameter for application requiring fast switching of output frequencies. Typical switching speeds range from 1 msec to about 10 μsec or less and synthesizers with switching speeds of less than 1 μsec have been built.

5) Spurious signals and noise:

Frequency synthesizer output is not a perfect sinusoid but is corrupted by other undesirable components. This is a measure of the synthesizer quality and can be divided into a) coherent spurious signals generated in the various nonlinear operations in the synthesis process and b) non-coherent noise outputs due to synthesizer circuit noises. This non-coherent noise is termed the phase noise and determines short term stability performance of the synthesizer. The spurious signals are specified by specifying the maximum power in db within a specified bandwidth related to the carrier power for all bandwidths offset from the carrier by a specified minimum frequency seperation.

6) Long term frequency stability:

The long term output frequency stability of a

synthesizer is dependent on the reference frequency source, and is defined usually, as the stability over one second or more averaging times used in the measurement. In synthesizer the reference is normally built-in and provision is made also to use higher quality external standard like an atomic frequency standard. The built-in reference is usually temparature controlled crystal oscillator with aging rates of less than 5 in 10^{16} parts per day and with less than 3 in 10^{9} parts variation in output frequency over 0 to 50°C (ambient temperature range.

7) Short term frequency stability:

Short term stability refers to the fluctuations in output frequency over averaging times less than 1 sec. This performance depends on the phase noise resulting from the synthesizer electronics. The short term stability can be characterized both in the frequency domain and in time domain.

3.2 Frequency Synthesis Techniques: [Ref. 7]

The synthesis schemes employed to realize a frequency synthesizer could be catagorised into four types viz. 1) In coherent Direct 2) Coherent Direct synthesis 3) Coherent Indirect synthesis and 4) All Digital frequency synthesis

schemes. The incoherent direct scheme is almost absolete. The remaining three schemes have their own favourable features and limitations and the choice depends upon the specifications. of the frequency synthesizer under development. The main difference between incoherent and coherent synthesis lies in the number of frequency sources utilized in the process of frequency synthesis. In the incoherent approach a number of independent crystal controlled oscillators are used and in the coherent approach only one reference is used. Hence the stability and accuracy of the output frequency in a coherent direct synthesis system are of the same order as the stability and accuracy of the single reference source. The feature that all frequencies are generated from a single reference source in the coherent scheme makes the coherent synthesis indispensible in a majority of situations. The all digital approach is limited to the low frequency spectrum and is therefore not employed in broad band high frequency synthesizers. However because of the precise and repeatable performance it delivers as a result of the digital manipulation of samples, it undoubtedly is a desirable approach for low frequency synthesis.

3.2.1 In-coherent Synthesis Scheme:

The block diagram of an incoherent synthesis approach is shown in Fig. 3.1. The synthesis utilizes the

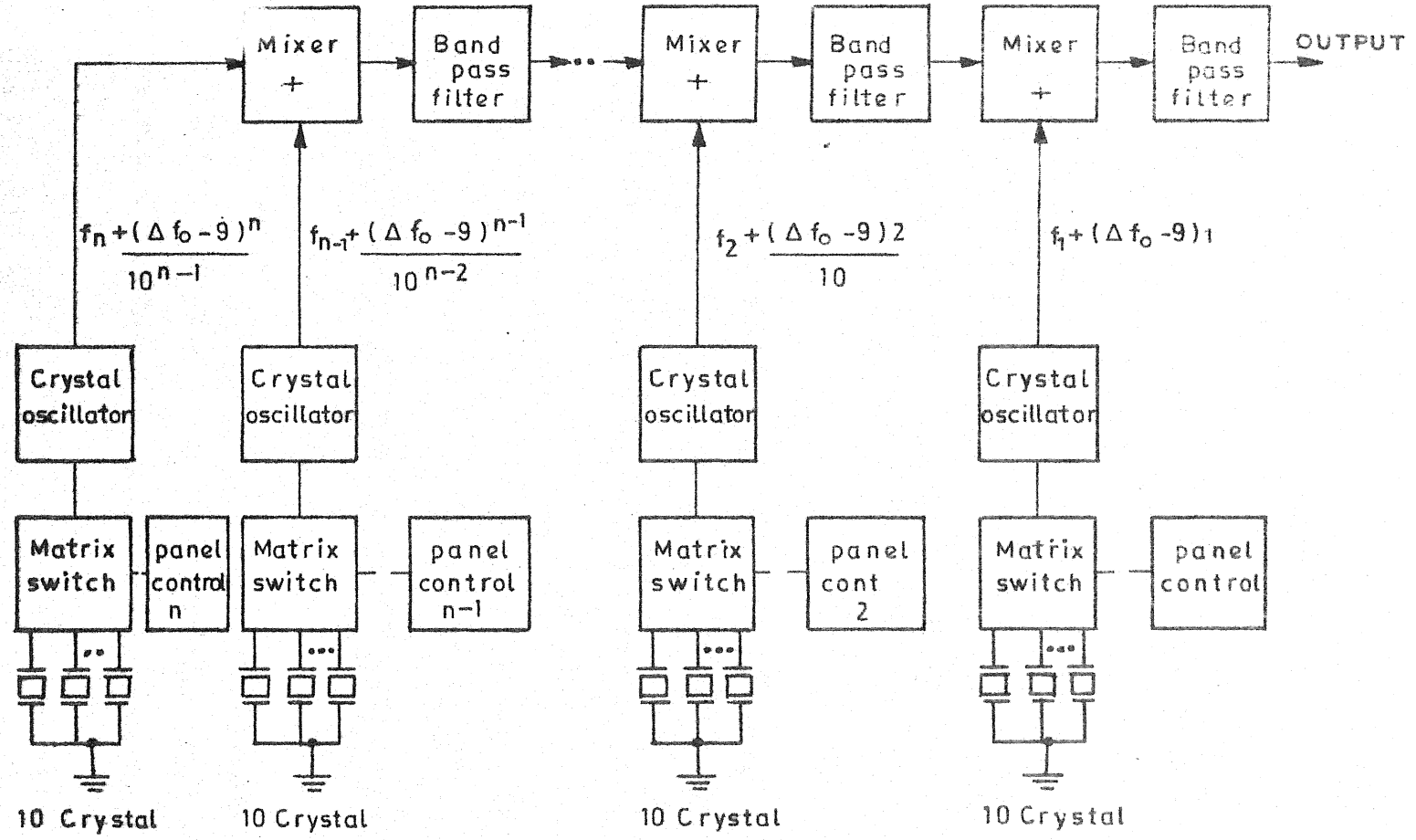


FIG.3.1 Incoheret synthesis scheme

method of successive heterodyning. The final output frequency can be shown to be

$$f_{out} = f_1+f_2+\ldots+f_{n-1}+f_n+(\Delta f_{o-9})_1+f(\Delta f_{o-9})_2 + \ldots + \frac{(\Delta f_{o-9})_{n-1}}{10^{n-2}} + \frac{(\Delta f_{o-9})_n}{10^{n-1}} \quad (3.1)$$

where $(\Delta f_{o-9})_n$ means that the nth stage the frequency can be switched to one of the ten frequencies .

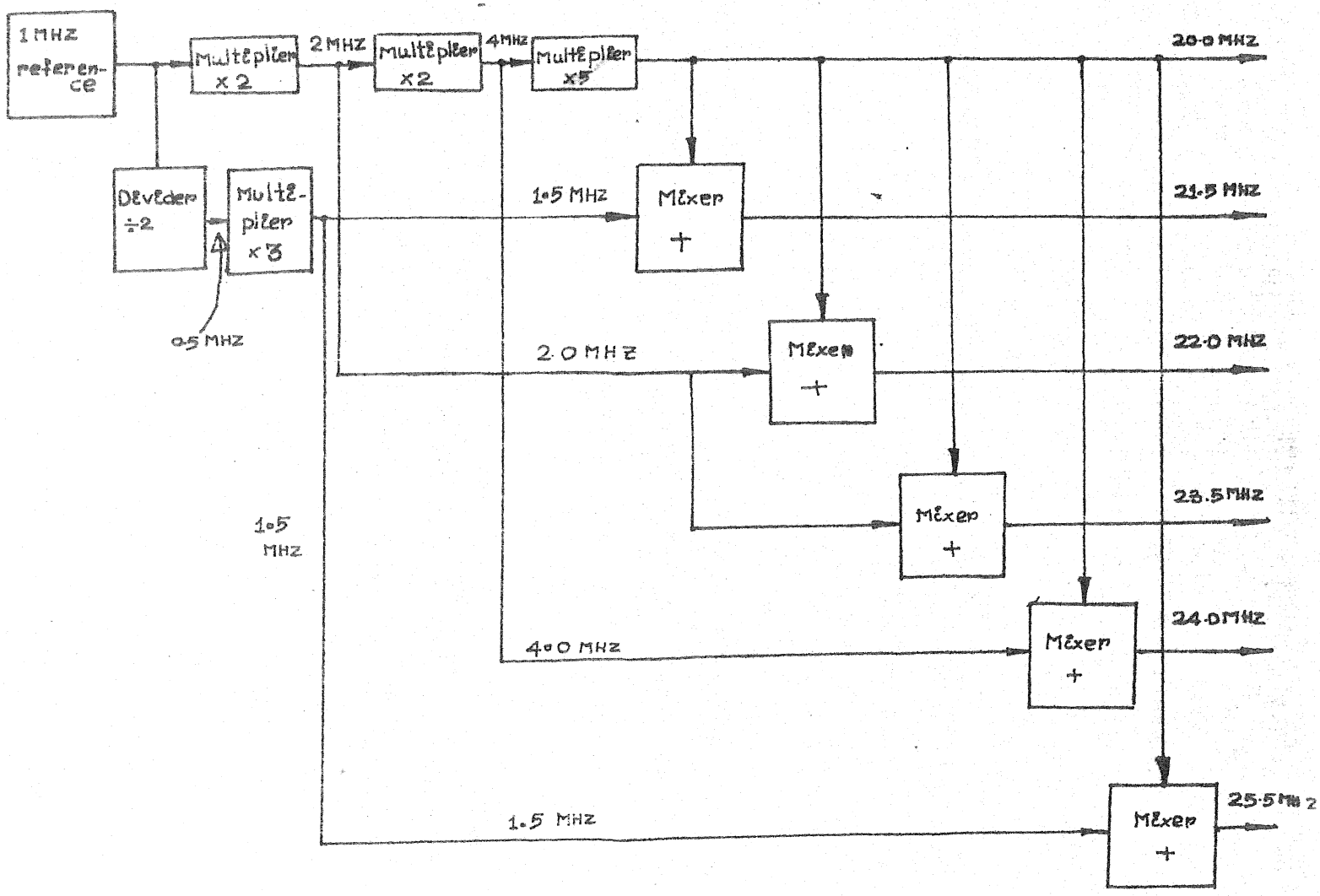
3.2.2 Coherent Direct Synthesis Scheme:

The coherent direct synthesis scheme could be further catagorized into two types viz. the brute-force approach and the harmonic approach. The brute-force approach is preferred whenever a small number of frequencies are to be generated simultaneously. The harmonic approach is preferred when the spacing between any two adjacent programmable output frequencies is the same number throughout the range and only single frequency output is to be provided at a time.

3.2.2.1 Brute-force approach:

The generation of six frequencies simultaneously using this approach is shown in Fig. 3.2. The basic building blocks in this approach are frequency multipliers, dividers, mixers and a reference source. Two problems associated with

Fig 3-2 Brute-Force Approach



brute-force approach are a) undesirable spurious outputs generated as a result of a number of mixing, multiplication and division operations, and b) phase noise around the output frequency.

3.2.2.2 Harmonic approach:

This approach consists of two basic steps a) generation of a signal with a high harmonic content whose fundamental frequency is equal to the output frequency spacing b) selection of desired harmonics. Three practical schemes of harmonic synthesis are shown in Fig. 3.3. In the figure the expression $\sum_{m=x_1}^{x_2} mf_r+R$ describes an input signal with a harmonic content. The harmonics of the signal that are passed by the filter, one at a time are x_1f_r through x_2f_r. The rest of the harmonics suppressed by the filter are denoted as R.

The passive filter in Fig. 3.3(a) is used to select harmonics whenever the spacing between the adjacent harmonics is large in relation to the output frequency, mf_r, so that required attenuation of unwanted harmonics is achieved with a small number of poles. When the spacing is small, the double-mix approach shown in Fig. 3.3(b) is used. In this approach a train of pulses is applied to the signal port of a difference mixer. Local oscillator input is provided by a

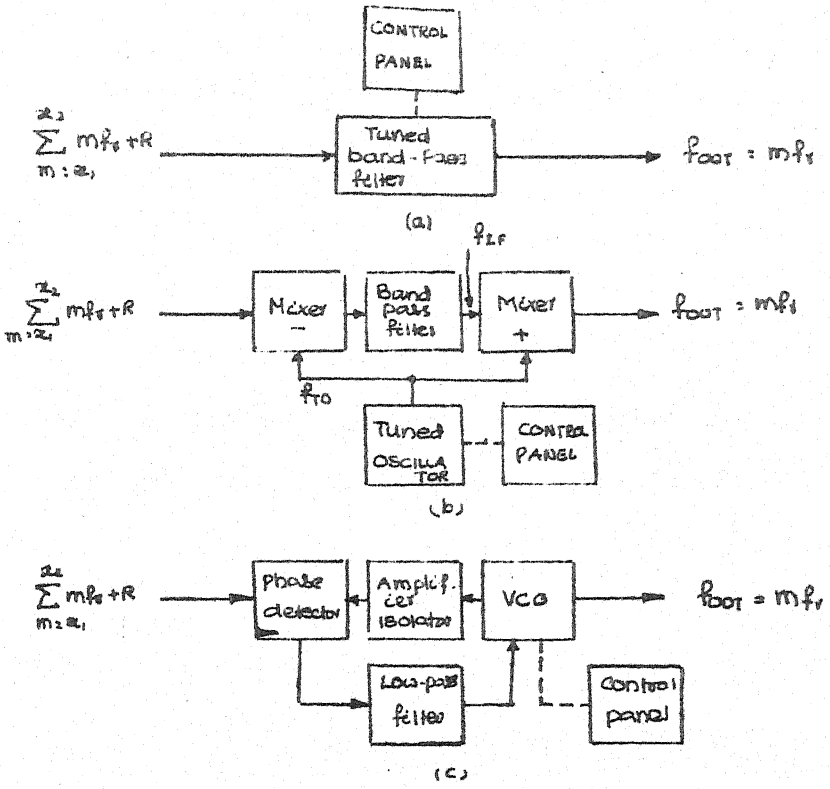


Fig 3.3 Harmonic synthesis (a) passive filter (b) Active filter, double-mix approach, (c) Active filter, phase-locked loop approach

tuned oscillator whose frequency, f_{TO}, is smaller than the output frequency, mf_r always by a fixed amount, f_{IF}. A band-pass filter following the mixer attenuates unwanted harmonics. The phase-locked loop approach, depicted in Fig. 3.3(c) is most useful when spacing between operating frequencies is so small that neither passive nor double-mix filters can attenuate unwanted harmonics.

3.2.3 Coherent Indirect Synthesis:

The coherent indirect synthesis utilizes principle of feed back in the form of a phase locked loop in generating wide range of frequencies from a single frequency reference. The system analysis of this technique centres on investigation of the phase locked loop stability and acquisition. The system components include voltage controlled oscillators, phase detectors, frequency discriminators and programmable dividers besides mixers, multipliers, dividers and filters which are the building blocks in the other synthesis schemes. Phase noise, switching speed,frequency increments and environmental performance differ from those displayed in direct synthesis. The performance of this scheme depends on the dynamics of the component phase locked loops. The scheme inturn renders itself into different implementations , each implementation employing a phase locked loop or a

number of phase locked loops in the process. This scheme renders small size, light weight, low D.C. power consumption and many other advantageous not offered by direct synthesis.

Any frequency synthesizer implementation employing phase locked loop falls under the coherent indirect synthesis. The phase locked loop may however be of the analog or digital types. The analog types employ sinusoidal phase detectors and voltage controlled oscillators. And the digital types employ digital logic compatible phase-frequency discriminators and voltage controlled oscillators. The advances in MSI technology has resulted in a wide range of IC's, specially suitable for digital frequency synthesis. These IC's have made ease and compact the construction of digital frequency synthesizers thereby increasing greatly their application potential. The synthesizers described in Chapter IV take full advantage of these MSI building blocks.

The theory of a phase locked loop fundamental to the coherent indirect frequency synthesis and the frequency synthesizers described in Chapter IV is briefly described in Section 3.3.

3.2.4 All Digital Frequency Synthesizer: (Ref. 6)

The tremondous advances made in the digital device technologies have rendered complete digital frequency

synthesis practical. The complete digital frequency synthesis approach uses the stable source frequency to define sampling times at which digital sinusoid sample values are produced. These samples are D/A converted and smoothed by some realizable linear filter to produce analog frequency signals. The frequency is determined by varying the amplitude of the samples and not by changing the sampling interval and is shown in Fig. 3.4. The digital synthesis consists of computing at some real time interval T, values of a desired phase angle, $w_o^t = w_o n^T$, with a desired synthesizer output frequency, and then using this value of phase angle to compute a sinusoidal output sample, $\sin w_o n^T$ in real time, since phase angle is a linear function of time and treated modulo 2π, a simple accumulator of phase increments, w_o^T, with overflow at effective 2π, solves the angle computation.

Assuming the smoothing filter presents no serious design problem and the D/A converter produces distorsion free analog samples, then a suitable technique for the digital sample value determination remains as the design problem.

Methods available to determine sine and cosine of some arguments, nwT, where n is a sample index, T the sampling interval, and w the desired frequency, are basically

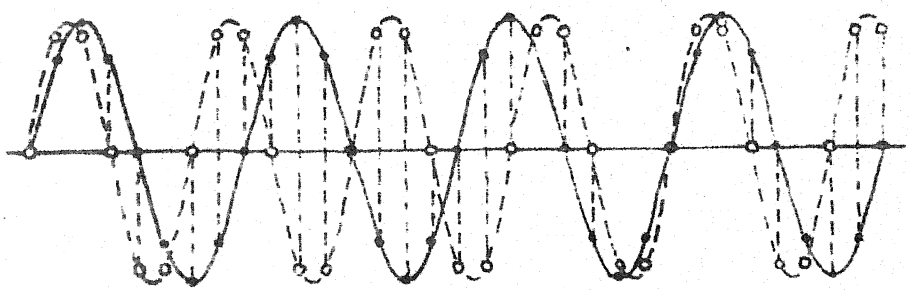


FIG 3.4 Digital Frequency Determination

1) Digital recursion oscillator
2) Direct computation based on some numerical approximation
3) Direct table look-up

3.3 Phase Locked Loop Frequency Synthesis:

Ease of programmability, better spectral purity, higher frequency, resolution, large output frequency range and less circuit complexity of digital phase locked loop frequency synthesizers, Lead the disigners to adapt this technique. In Chapter IV, the RF programmable chirp frequency synthesizer designed and developed using this technique, is described in detail.

3.3.1 The Phase Locked Loop:

The phase locked loop is a closed-loop electronic servo whose output locks on to and tracks an input reference signal. Phase lock is obtained by comparing the phase of the output signal with that of the reference, and any phase difference is converted into an error correction voltage. This error voltage changes the output signal phase to make it track the input. The servo system has three basic partitions; a phase detector, a loop filter, and a voltage controlled oscillator.When the phase difference

between the VCO and the input reference signal is constant, the loop is locked. If either the reference or the VCO output changes phase, the phase detector and filter produce a d.c. error voltage proportional in magnitude and polarity to the signal phase change. This error voltage changes the phase of the VCO by altering its frequency, which locks it on to the reference signal. When a programmable frequency divider is inserted in to the feed back path of the phase locked loop as shown in Fig. 3.5, the output frequency becomes an integral multiple of the reference frequency. This technique is used for multiple frequency generation in frequency synthesizers. The equation describing the output frequency is

$$f_o = Nf_r \qquad (3.2)$$

In the following section the analysis of the phase locked loop is carried and the design equations are developed.

3.3.1 PLL analysis:

The basic phase locked loop (Fig. 3.5) can be modelled as shown in Fig. 3.6(a).

If we choose a second order loop filter, then K_F = Amplifier/Filter gain is given by

$$K_F = \frac{1 + T_1 s}{T_2 s} \qquad (3.3)$$

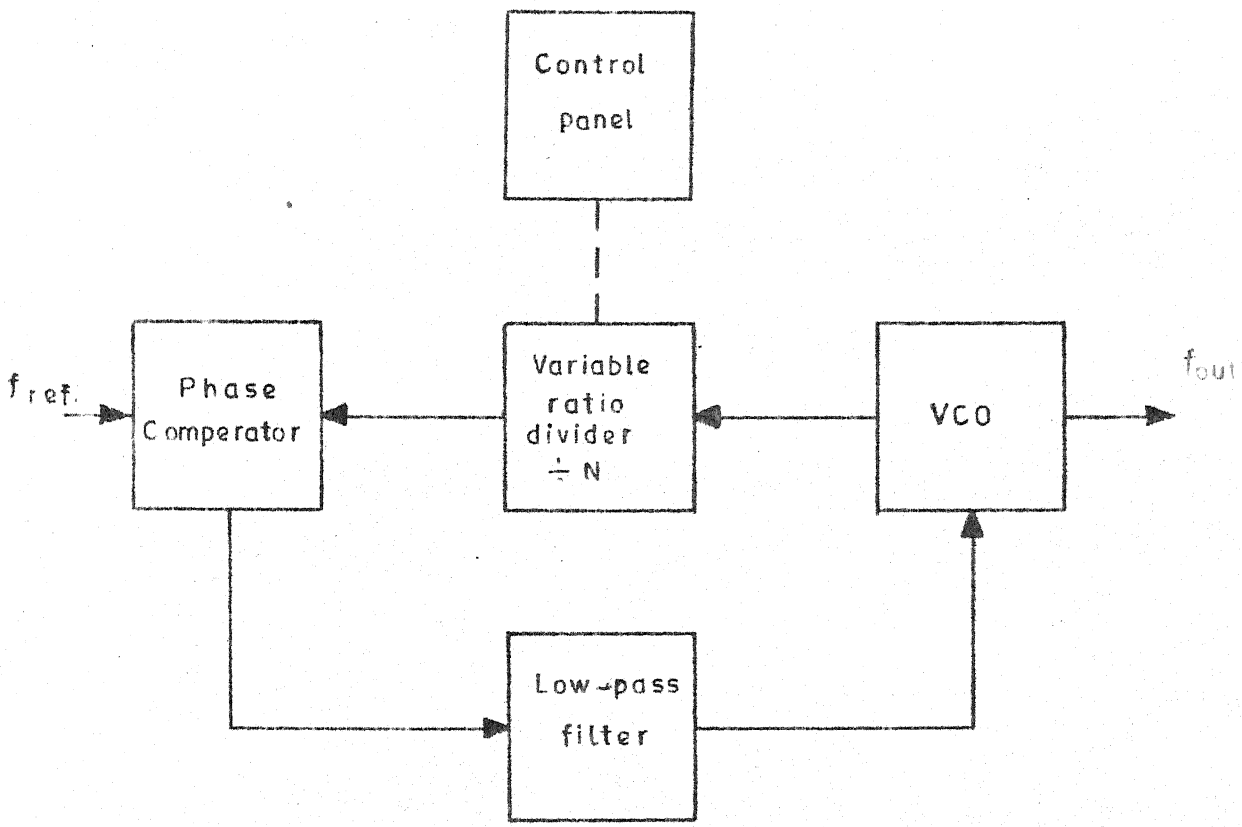
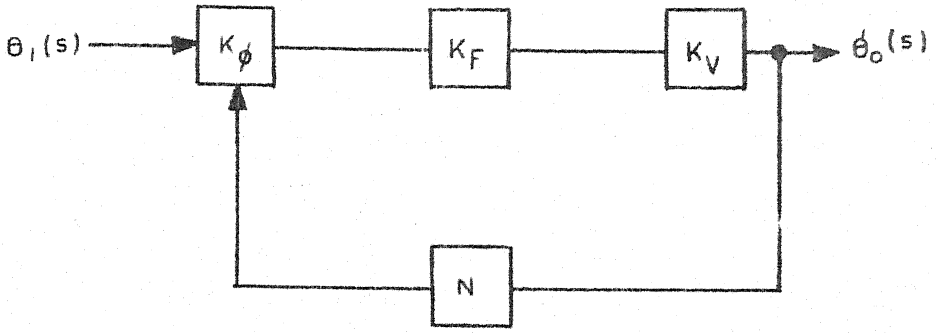


FIG.3.5 Phase locked loop.



K_ϕ = Phase Detector Gain (volts radian)

K_F = Amplifier/Filter Gain

K_V = VCO Gain (radians/second/volt

N = Integer Divisor

FIG 3.6(a) PLL Model

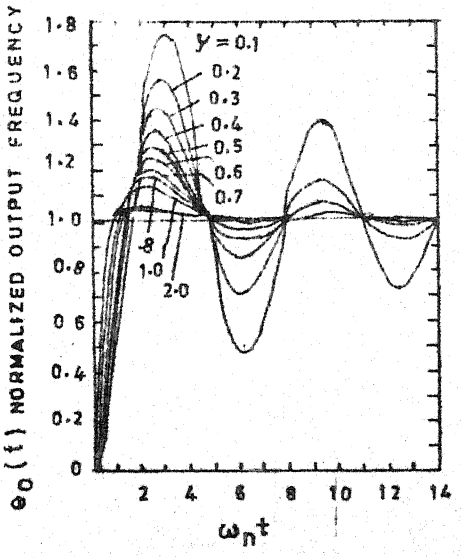


FIG. 3.6(b) Type 2 Second order step response

$T_1 = R_2C$ and $T_2 = R_1C$ (Ref. Fig. 4.7)

Now the transfer function is given by:

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{K_\phi K_F K_V}{s + \frac{K_\phi K_F K_V}{N}} \qquad (3.4)$$

Substituting (eqn. (3.3) in eqn. (3.4), we get

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{N(1 + T_1 s}{\frac{s^2 N T_2}{K_\phi K_V} + T_1 s + 1} \qquad (3.5)$$

This can be simplified in the form of a second order system and identify parameters like loop bandwidth (w_n) and the damping factor (δ)

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{\frac{N(1+ T_1 s)}{N T_2}}{s^2 + T_1 s\left(\frac{K_\phi K_V}{NT_2}\right) + \left(\frac{K_\phi K_V}{NT_2}\right)} \qquad (3.6)$$

From eqn. (3.6), $w_n = \sqrt{\frac{K_\phi K_V}{NT_2}}$ (3.7)

$$\delta = \sqrt{\frac{K_\phi K_V}{NT_2}} \left(\frac{T_1}{2}\right) \qquad (3.8)$$

Hence eqn. (3.6) can be simplified as;

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{N(1+T_1 s)}{\frac{s^2}{w_n^2} + \frac{2\delta s}{w_n} + 1} \qquad (3.9)$$

The response of this second order system for a step input is shown in Fig. 3.6(b). Constants K_ϕ, K_V and N are usually fixed due to other design constraints, leaving T_1 and T_2 as variables to set w_n and δ. Since only T_2 appears in eqn. (3.7) it is the easiest to solve for initially.

$$T_2 = \frac{K_\phi K_V}{N w_n^2} \qquad (3.10)$$

From equation (3.8), we find

$$T_1 = \frac{2\delta}{w_n} \qquad (3.11)$$

using eqn. (3.10) and eqn. (3.11) actual resistor values may be computed:

$$R_1 = \frac{K_\phi K_V}{N w_n^2 C} \qquad (3.12)$$

$$R_2 = \frac{2\delta}{w_n C} \qquad (3.13)$$

In the next chapter the above equations are used in the design of RF programmable chirp synthesizer.

CHAPTER IV

PROGRAMMABLE RF CHIRP SYNTHESIZER DESIGN

The design and fabrication of RF programmable chirp frequency synthesizer is described in the following sections. Fig. 4.1 shows the block diagram of RF chirp Synthesizer as well as its carrier frequency generation.

In Fig. 4.1, PLL-1 generates frequencies from 20 to 60 MHz in steps of 10 KHz. PLL-2 generates chirp signal on a 60 MHz carrier. PLL-3 generates the 60 MHz carrier frequency. At the output of the Mixer -1,by selecting the lower side band we will get the frequencies from 0 - 40 MHz in steps of 10 KHz with a chirp deviation of 10 KHz. And at the output of Mixer-2 we will get the carrier frequencies from 0 - 40 MHz in steps of 10 KHz. Outputs of Mixer - 1 and Mixer-2 are sufficiently amplifi ed and bufferd before giving to the system under test and phase sensitive detector respectively. In the following section the design of programmable frequency synthesizer is carried out.

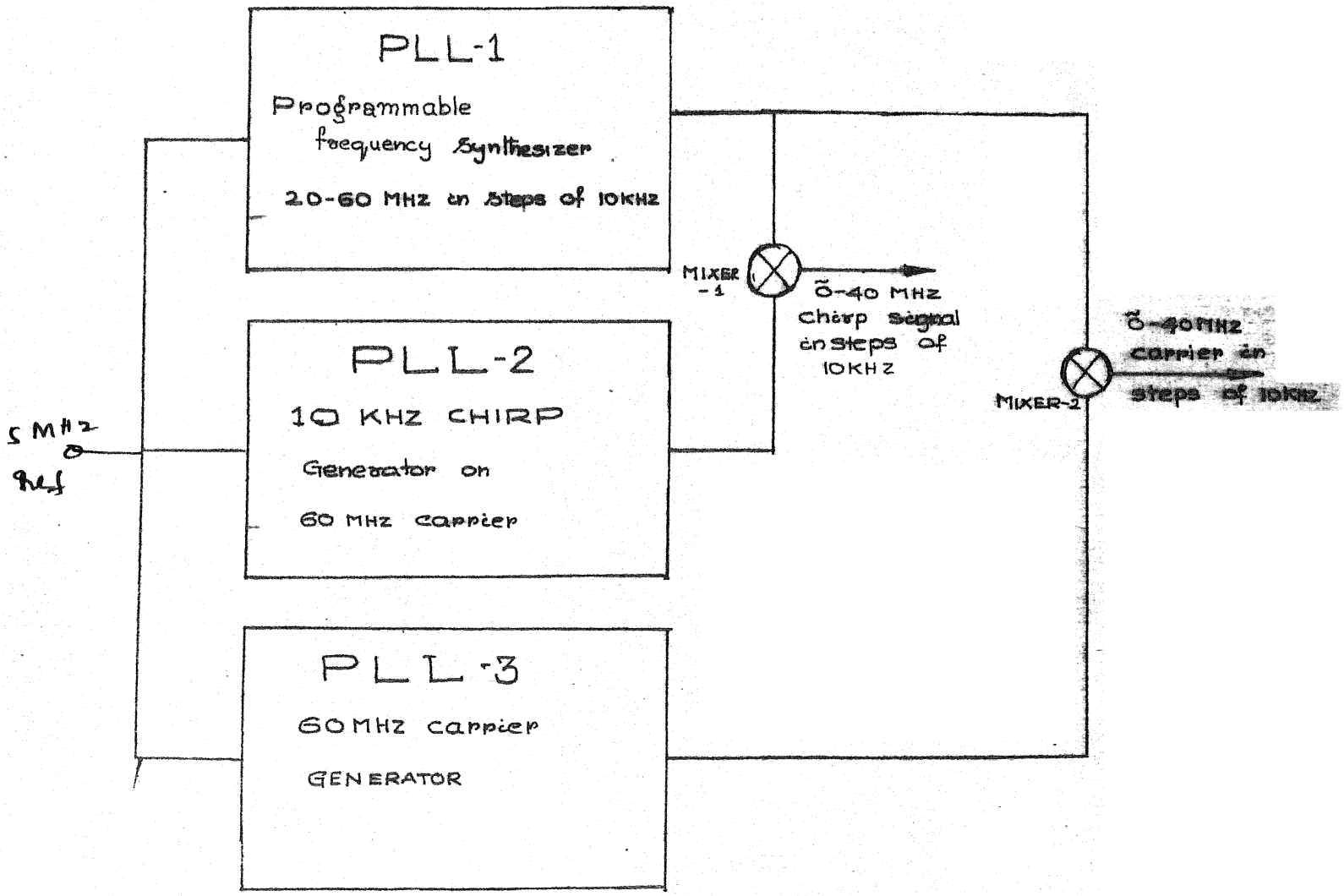
4.1 Programmable Frequency Synthesizer :

4.1.1. Specifications :

The following are the specifications aimed at in designing the programmable frequency synthesizer.

1) Output frequency range - 20-60 MHz.

Fig 4.1 RF Programmable Chirp Synthesizer



2) Number of channels - 4000.

3) Channel spacing - 10 KHz.

4) Switching time - is not important for the present application.

5) Stability - 1 part in 3×10^6

4.1.2. The block schematic of programmable frequency synthesizer is shown in Fig. 4.2. Motorola chips are selected for the purpose of voltage controlled oscillator (MC 1648), phase detector (MC 4044) and programmable counters(MC 4016). Hence for the design, data is taken from the Motorola application notes. (Ref.8).

Step 1 :

The circuit schematic and the circuit configuration of MC 1648 used in this design are shown in Fig. 4.3(a). The design equations for the calculations of inductance and varacter capacitance can be derived as :

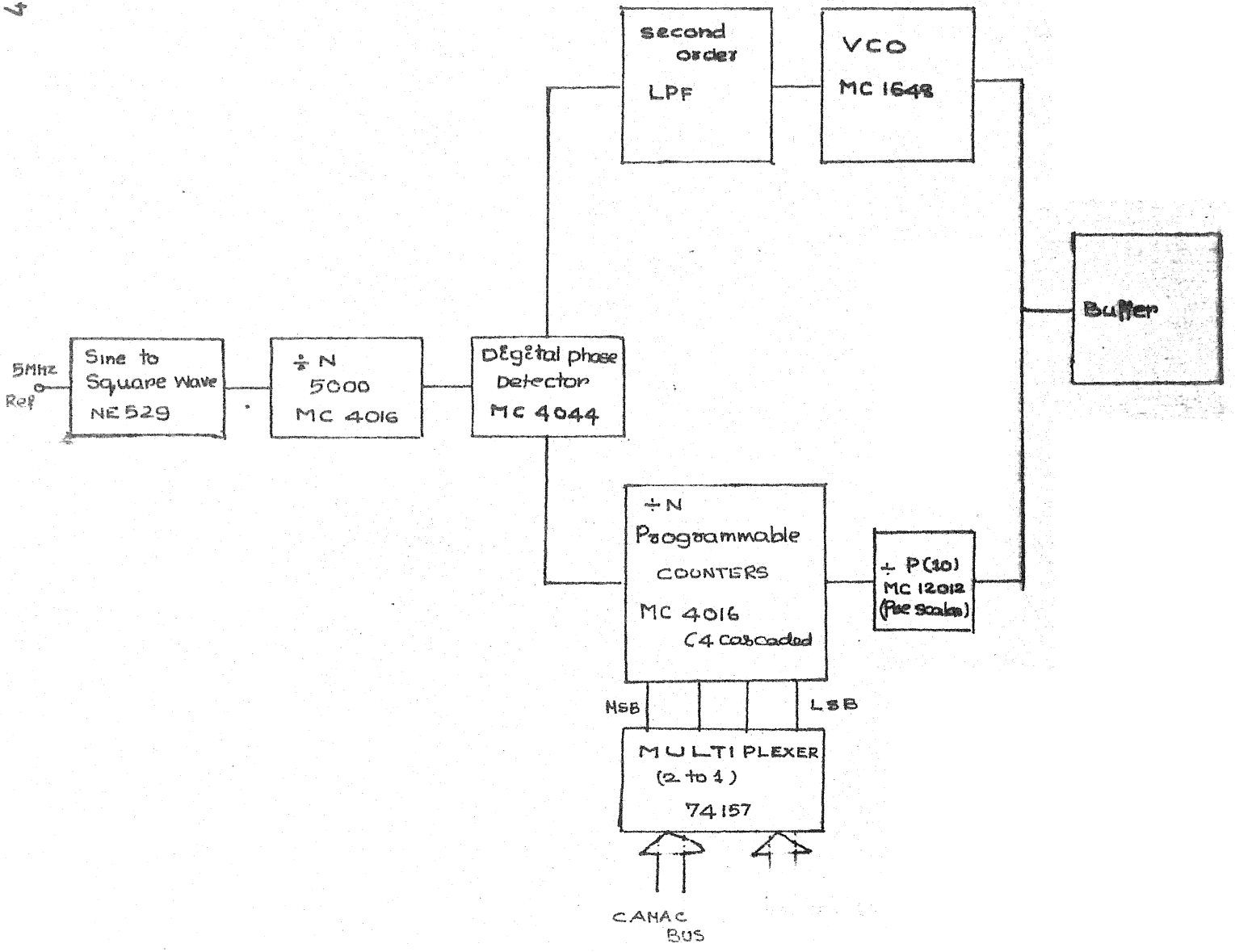
$$\frac{f_{max}}{f_{min}} = \sqrt{\frac{C_D(max) + C_S}{C_D(min) + C_S}} \qquad (4.1)$$

where

f_{max} = VCO maximum frequency.

f_{min} = VCO minimum frequency.

Fig 4.2 Programmable frequency Synthesizer



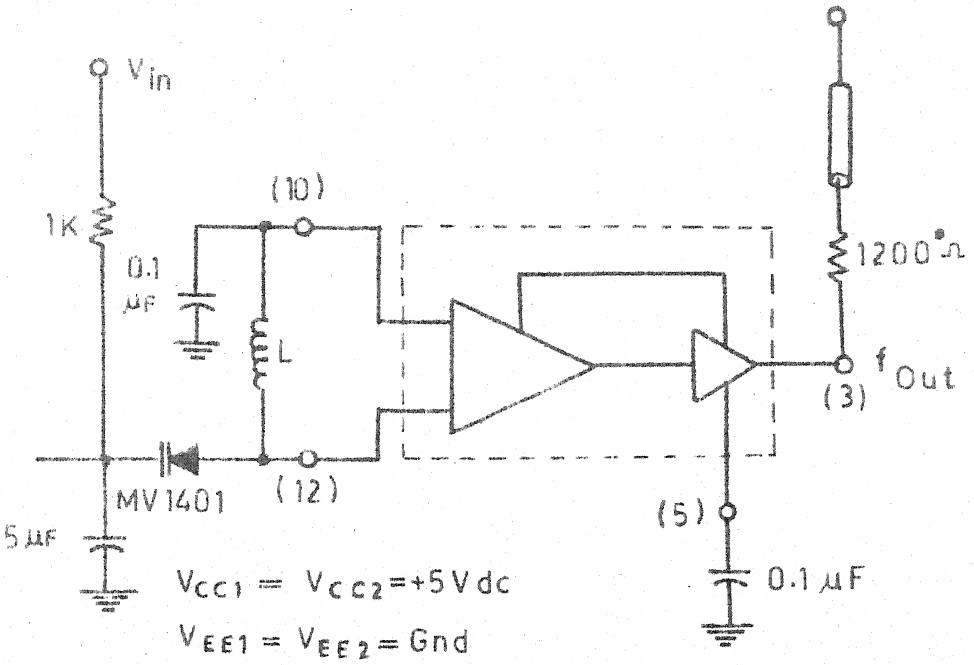


FIG.4.3 (a) V.C.O. Circuit schematic

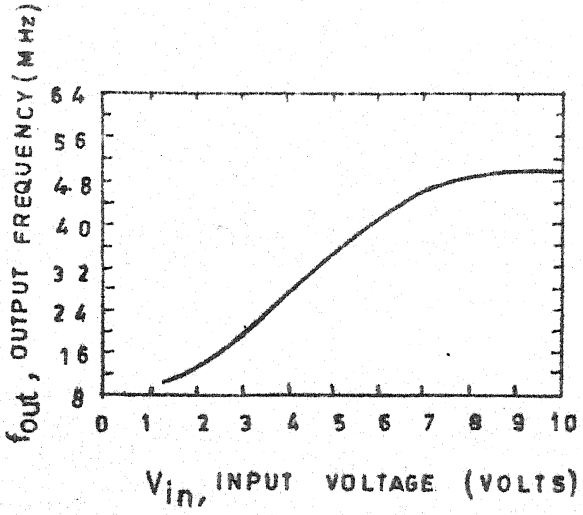


FIG. 4.3 (b) V.C.O. Transfer characteristic

C_D (max) = varactor diode maximum capacitance

C_D (min) = " " minimum capacitance.

C_S = MC 1648 input capacitance + any external capacitance if added.

$$f_{min} = \frac{1}{2\pi\sqrt{L\,(C_D\,(max) + C_S)}} \qquad (4.2)$$

In equation (4.2) the value of inductance (L) is chosen in such a way that the capacitance variation required is in the order of 20 pF to 250 pF which facilitates the use of available varactor diodes.

If we choose L as 0.10μH, then C_D (max) + C_S can be calculated as follows

From eqn. 4.2;

$$C_D\,(max) + C_S = \frac{1}{4\pi^2 (f_{min})^2 L}$$

$$= \frac{10^{12}}{4 \times 6.28 \times (20\times10^6)^2 \times 0.10 \times 10^{-6}} \text{ pF} = 160\text{pF}$$

C_S = Input capacitance + external capacitance

The input capacitance of MC 1648 is 6 pF and if we choose C_S (external) as 0pF then

$$C_D \text{ (max)} = 160 - 06 = 154 \text{ pF}$$

From eqn (4.1); we know f_{max} = 60 MHz & f_{min} = 20 MHz

$$\frac{f_{max}}{f_{min}} = \frac{60}{20} = 3 \qquad (4.3)$$

Now from equations (4.1), (4.2) & (4.3) : C_D(min) can be calculated

$$C_D \text{ (min)} = \frac{(C_D(\text{max}) + C_S)}{\left(\frac{f_{max}}{f_{min}}\right)^2} - C_S$$

$$= \frac{160}{9} - 6 = 11\text{pF}$$

The above designed variation in varactor capacitance can be obtained by the MV 1404 varactor diode. From the transfer characteristics of MV 1404 the required voltage can be noted as : 1.0 to 6.0 volts.

Step 2 : Reference frequency selection :

The output frequency of the PLL is given by

$$f_0 = Np\, f_r \qquad (4.4)$$

where

N = programmable counter divisor

P = prescalar divisor

f_r = reference frequency

The maximum frequency of operation of the programmable counters is limited to 8 MHz. Hence the minimum divisor required for prescalar is given by

$$P_{min} = \frac{f_{out}\ (max)}{8\ MHz} = \frac{60}{8} \simeq 8$$

P_{min} will be chosen as 10; as MC 12012 prescalar chip has provision for 10

Hence from equation (4.4) $f_o = 10N\ f_r$. This shows that for each increment in N the output frequency is multiplied by ten times f_r. As per specifications stated the channel spacing is 10 KHz. Hence the reference frequency is given by

$$f_r = \frac{\text{channel spacing}}{10} = 1\ KHz$$

Step 3 : Programmable counters :

From equation (4.4) the minimum and maximum division required for programmable counters can be found as

$$N_{min} = \frac{f_o\ min}{Pf_r} = 2000$$

$$N_{max} = \frac{f_o(max)}{Pf_r} = 6000$$

The realisation of this programmable counter can be done by cascading four stages of MC 4016 programmable counters. The data will be entered into the MC 4016 programmable counters either CAMAC bus or by BCD thumb-wheel switches through a multiplexer. A two to one multiplexer is realised using four 74157 for four digits.

Step 4: Phase sensitive detector :

Digital phase frequency detection is obtained by using MC 4044 phase sensitive detector. The circuit schematic of MC 4044 phase sensitive detector is shown in Fig. 4.4. Fig. 4.4 shows the block diagram of phase-frequency detector. Fig. 4.4.a shows the circuit schematic of phase detector 1. Fig. 4.4(b&c) shows circuit schematic of charge pump and amplifier. Fig.4.5(a) shows the truth table of phase frequency detector 1 and Fig. 4.5(b) shows the timing diagram. Fig. 4.6(a) shows the circuit schematic of phase detector 2, Fig. 4.6(b) shows the truth table and Fig. 4.6(c) shows the timing diagram. It is easily observed from the timing diagrams of phase detector 1 and 2 that the phase detector 1 detects the phase and frequency between Reference and variable inputs and phase detector 2 detects only phase difference between reference and variable inputs .So in the present application the phase detector 1 is used to detect the phase and frequency and phase detector 2

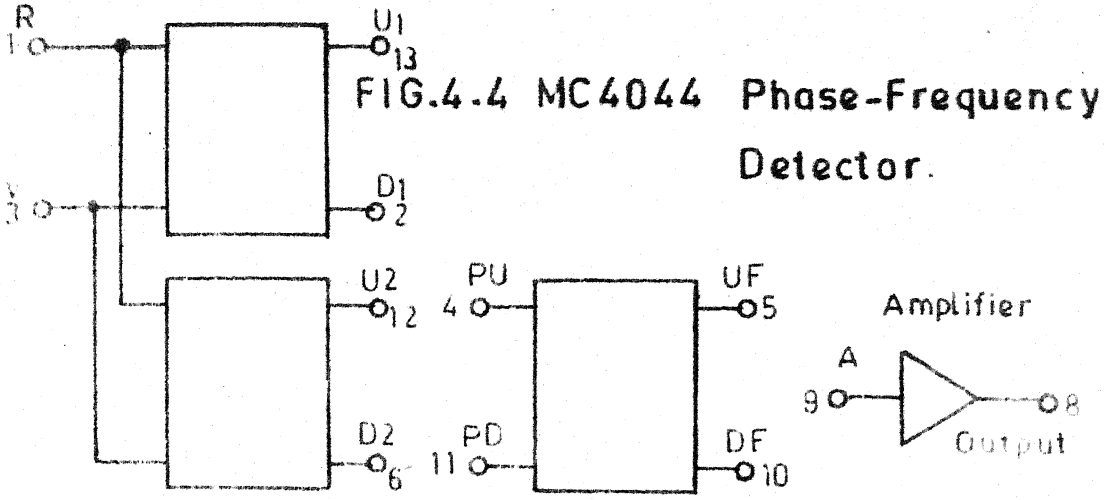


FIG.4.4 MC4044 Phase-Frequency Detector.

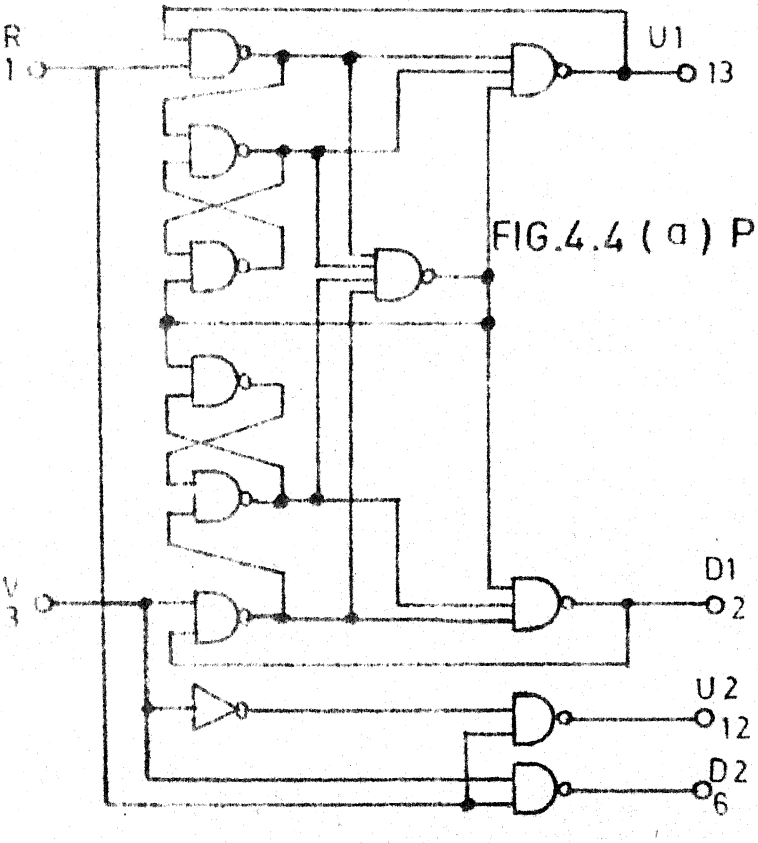


FIG.4.4 (a) Phase Detector

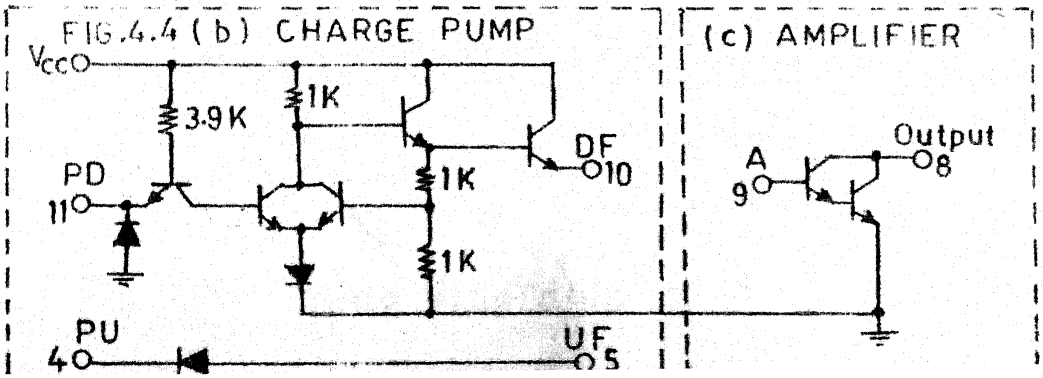
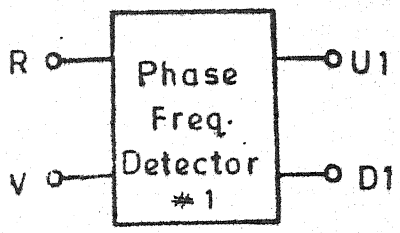


FIG.4.5 (a) Truth table



R.V 0.0	R.V 0.1	R.V 1.1	R.V 1.0	U1	D1
(1)	2	3	(4)	0	1
5	(2)	(3)	8	0	1
(5)	6	7	8	1	1
9	(6)	7	12	1	1
5	2	(7)	12	1	1
1	2	7	(8)	1	1
(9)	(10)	11	12	1	0
5	6	(11)	(12)	1	0

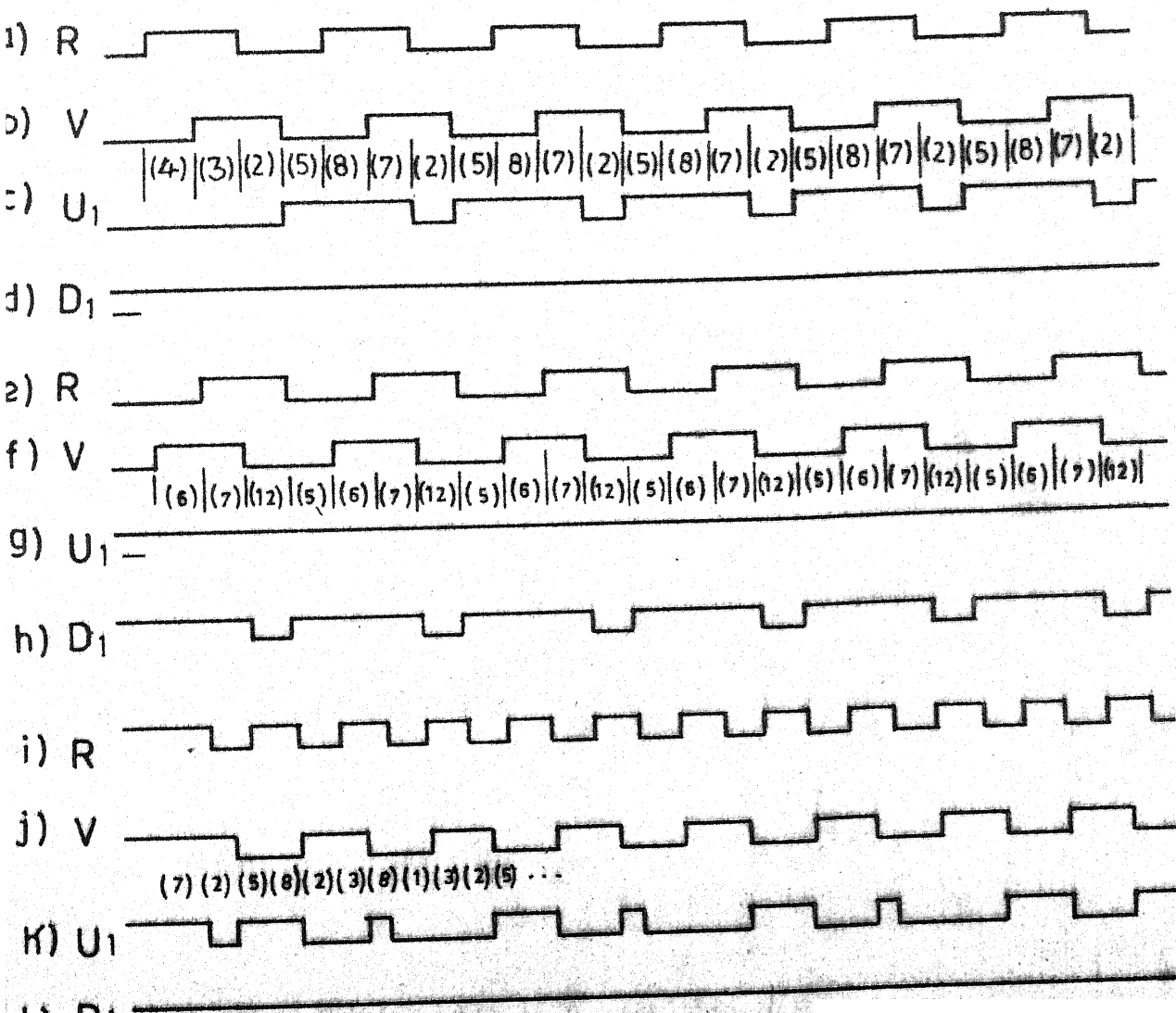


FIG.4.5 (b) Timing diagram.

FIG.4.5 Timing diagrams of MC4044.

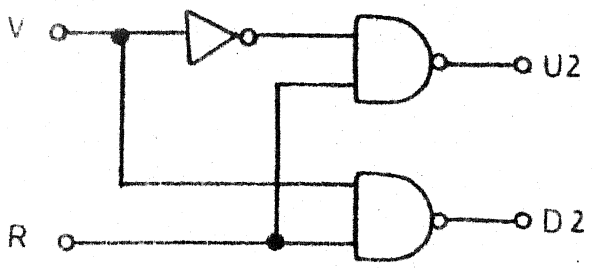


FIG.4.6(a) Phase detector

Truth Table

R	V	U2	D2
0	0	1	1
0	1	1	1
1	0	0	1
1	1	1	0

FIG.4.6(b) Truth table

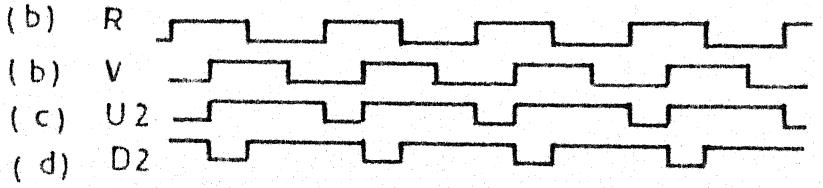


FIG.4.6 (c) Timing diagram

FIG.4.6 MC4044 Phase detector 2

is used as lock in indicator. The charge pump followed by phase detector 1 serves as level translator as well as to give pump up and pump down signals. The output of the charge pump will be 2.25 volts for pump up signals, and 0.75 V for pump down signals. Hence the phase detector gain constant is 0.12 volt/ radian.

Step 5: Loop Filter :

The design of loop filter is so critical that the fundamental loop characteristics such as capture range, loop band width, switching time and spurious side bands are controlle primarily by the loop filter. The analysis of PLL using second order loop filter is described in Chapter III and hence forth the following design equations are taken from Chapter III for the design of loop filter. The second order loop filter schematic is shown in Fig. 4.7.

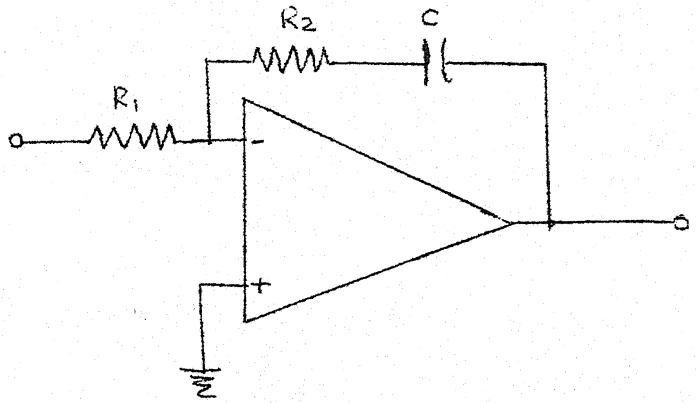


Fig. 4.7 Loop filter

The transfer function of this filter is given by

$$K_F = \frac{1 + T_1 s}{T_2 s} \qquad (4.5)$$

where

$$T_1 = R_2 c \text{ and } T_2 = R_1 c \qquad (4.5(b))$$

Loop band width or natural frequency w_n is given by

$$w_n = \sqrt{\frac{K_\phi K_V}{N T_2}} \qquad (4.6)$$

where

K_ϕ = phase detector gain, K_V = V CO gain

and $N = N_{max}, T_2 = R_1 C$

The damping δ is given by

$$\sqrt{\frac{K_\phi K_V}{N T_2}} \left(\frac{T_1}{2} \right) \qquad (4.7)$$

Loop band width $w_n = \frac{w_n t}{t}$ (4.8)

Capacitor $C = \frac{K_\phi K_V}{N_{max} w_n^2 R_1}$ (4.9)

$$R_2 = \frac{2 \delta_{min}}{w_n C} \qquad (4.10)$$

Refer to Fig. 3.6(b), type 2 second order step response with $\delta = 0.8$, over shoot will settle to with in 5% at $w_n t = 4.5$. Since the reference frequency is 1 KHz, the loop band width w_n is chosen as 100 Hz to reduce reference feed through to a tolarable value.

The lock up time is given by: $t = \frac{w_n t}{w_n}$ (4.11)

$$t = \frac{4.5}{100} = 45 \text{ m sec.}$$

Now the capacitance c can be calculated as;

Refering to Fig. 4.3(b), $K_V = 8 \times 10^6$, and from section 4.1.2 step 4, $K_0 = 0.12$ V/radian.

$$C = \frac{K_\phi K_V}{N_{max} w_n^2 R_1}$$

Choose $R_1 = 3.3$ KΩ, then

$$C = \frac{0.12 \times 8 \times 10^6}{60000 \times (100)^2 \times 3.3 \times 10^3} = 0.5 \mu F$$

and $$R_2 = \frac{2\delta}{w_n c} = \frac{2 \times 0.8}{100 \times 0.5 \times 10^{-6}} = 32 \text{ K}\Omega$$

The above designed values are the starting values for a loop filter. One has to optimise these values by testing the

circuit with the above initial values. This is due to various approximations in deriving the equations and also the constants used are not constant throughout the frequency of operation. For example K_V is not const through out the frequency range of interest.

Step 6 : Additional circuit design to reduce spurious outputs:

In the following paragraph the theory of spurious outputs design equations and necessary circuits to reduce the spurious outputs is discussed.

Although the major problem in phase locked loop design is defining loop gain and phase margin under dynamic operating conditions, high quality synthesizer designs also require special considerations to minimize spurious spectral components- the worst of which is reference frequency sidebands. Requirements for good sideband suppression often conflict with other performance goals. loop dynamic behaviour, suppression of VCO noise. As a result, most synthesizer designs require compromised specifications. For a given set of components and loop dynamic conditions, reference sidebands should be predicted and checked against design specifications before any hard ware is built. Any steady state variations on the V.C.O control line will produce sidebands in accordance with normal FM theory. For small

spurious deviations on the VCO relative sideband to carrier levels can be predicted by

$$\frac{\text{Sidebands}}{\text{carrier}} = \frac{V_{ref}\, K_V}{2\, w_{ref}} \qquad (4.12) \quad \text{(Ref.8)}$$

where V_{ref} = Peak voltage value of spurious frequency at the VCO input

Unwanted control line modulation can come from a variety of sources, but the most likely cause is phase detector pulse components feeding through the loop filter. Although the filter does establish loop dynamic conditions, it leaves something to be desired as a low pass section for reference frequency components. For the usual case where w_{ref} is higher than $1/T_2$, the K_F function amounts to a simple ratio.

$$K_F\,(jw)\Big|_{w\,=\,w_{ref}} \simeq -\frac{R_2}{R_1} \qquad (4.13)$$

Using eqn (4.9) and (4.10) for R_1 & R_2 this signal transfer function can be related to loop parameters.

$$K_F\,(jw)\Big|_{w=\,w_{ref}} \simeq \frac{2\,\delta_N\, w_n}{K_\phi\, K_V} = \frac{V_{ref}}{V_\phi} \qquad (4.14)$$

where

V_{ref} = Peak value of reference voltage at the V.C.O input

V_{ϕ} = Peak value of reference frequency voltage at the phase detector output.

Side band levels relative to reference voltage at the phase detector output can be computed by combining the equations (4.6) & (4.14).

$$\frac{\text{Sideband level}}{f_{out}\ \text{level}} = V_{\phi}\left(\frac{\delta N\, w_n}{w_{ref}\, K_{\phi}}\right) \qquad (4.15)$$

From equation (4.15) we find that for a given phase detector, a given value of R_1 (which determines V_{ϕ}) and given basic system constraints (N, f_{ref}), only δ and w_n remain as variables to diminish the sidebands. If there are few limits on w_n, it may lowered indefinitely until the desired degree of suppression is obtained. If w_n is not arbitrary and the sidebands are still objectionable, additional filtering is indicated. The equation 4.15 can be further simplified as follows. Refering to Fig. 4.8; in computing sideband levels, the value of V_{ϕ} must be determined in relation to other loop components. Residual reference frequency components at the phase detector output are related to the dc error voltage necessary to supply charge pump leakage current and amplifier bias current. From these average voltage figures, spectral components of the

reference frequency and its harmonics can be computed using an approximation that the phase detector output consists of square waves τ seconds wide repeated at t second intervals. The following observations can be made from the Fig. 4.8.

1) The average voltage (V_{avg}) is A τ/t
2) The peak reference voltage value V_{ϕ} is twice V_{avg} and
3) The second harmonic 2 f_{ref} is roughly equal in amplitude to the fundamental.

Since $V_{\phi} = 2\ V_{avg}$

$V_{avg} = (I_b + I_L)\ R_1$

$V_{\phi} = 2\ (I_b + I_L)\ R_1$

$V_{ref} = V_{\phi}\ (R_2/R_1)$

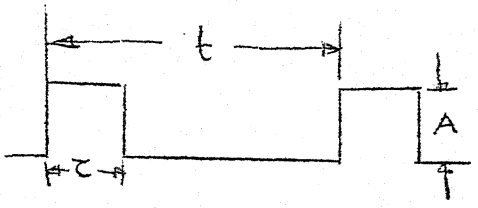


Fig. 4.8. Phase detector output

Hence $V_{ref} = 2\ R_1\ (I_b + I_L)\ \frac{R_2}{R_1} = 2\ R_2\ (I_b + I_L)$

using equation 4.12 we get $\frac{\text{Sideband}}{f_{out}} = \frac{2R_2\ (I_b + I_L)\ K_V}{2\ w_{ref}}$ (4.16)

Equation (4.16) indicates that excellent suppression could be achieved if the bias and leakage terms were nulled by current summing at the amplifier input. The possible circuit schematic compensating for bias and leakage currents is shown in Fig.(4.9).

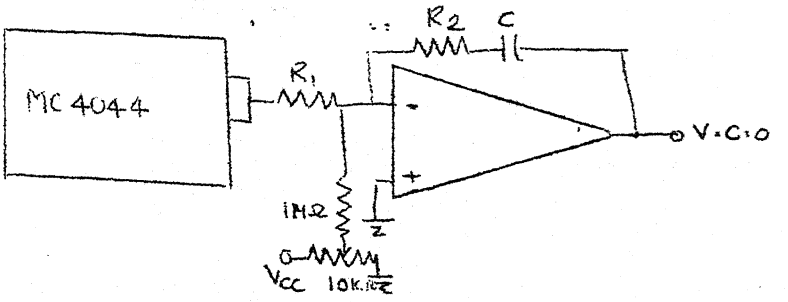
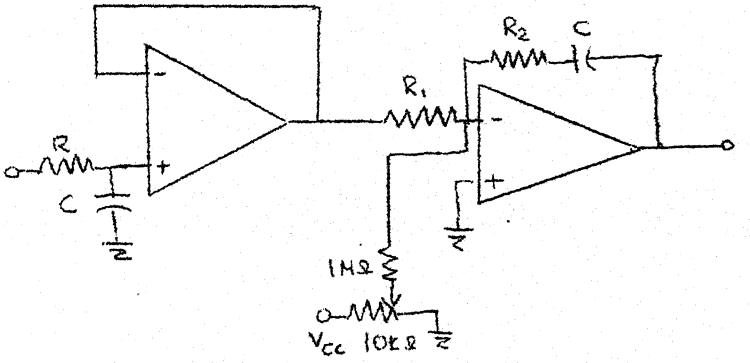


Fig. 4.9 Bias compensation

Further improvements in suppression will be accomplished by using a low pass section as shown in Fig. 4.10 preceeded to the loop filter.

The designed equations for R & C are as follows :

$$R\,C \simeq \frac{0.8}{w_n} \qquad (4.17) \qquad \text{(Ref. 8)}$$



4.10. Additional pole adding to the loop filter

Choose $C = 1\ \mu F$

Hence $R = \frac{0.8}{w_n C} = \frac{0.8}{100 \times 0.1 \times 10^{-6}}$

$R = 8\ K\Omega$

In the next section the design of chirp synthesizer is discussed.

4.2 Chirp Synthesizer :

In the following subsections the design of chirp synthesizer for three different chirp widths (Δf) viz$<$5 KHz , $<$10 KHz, $<$1 MHz is discussed. Phase locked loop is used to generate the carrier frequency of the chirp synthesizer. We know that any variation in the control line of VCO will lead to FM. Using this fact one can apply a ramp input at the control input to get a linear FM at the output assuming the VCO transfer function is linear in the operating range.

4.2.1. Specifications :

1. Carrier frequency : 60 MHz
2. Chirp width (Δf) : case 1) $<$5KHz
   2) $<$10 KHz
   3) $<$1 MHz

3. Chirp rate, chirp width and chirp frequency should be controllable.

4. Stability: The carrier frequency stability should be 1 part in 10×10^{6}Hz.

4.2.2 Design :

The step by step design procedure of a phase locked loop has all ready been dealt with in the previous section. The same procedure will be adopted for the design of 60 MHz carrier frequency of the chirp synthesizer using PLL except V.C.O. The design of V.C.O is carried in this section.

The circuit schematic of voltage controlled oscillator is shown in fig. 4.11(a) & (b) for the case of chirp width $(\Delta f) < 5$KHz. For narrow band chirping VCXO is prefered because of the following reasons 1) K_V the transfer gain of the VC xO is very low as compared to the other VCO's. Low transfer gain VC x O prevents to a minimum the output frequency variation due to noise. This point will be clear if we consider the gain of MC 1648 VCO. which needs roughly 1 mV to get 10 KHz variation in the frequency. 2) To facilitate chirping in PLL the loop time constant will be far greater than the chirp sweep time. This condition leads to stability and spurious outputs in the conventional VCO whose short term stability is poor compare to VC xO.

Fig. 4.11(a) is grounded base crystal oscillator (Ref.9). Between A & B the crystal is inserted to stabilise the oscillations. The tank circuit is tuned to 60 MHz. Capacitors C_1 and C_2 are selected to provide sufficient feed back for the

FIG 4.11(a) Grounded-base Oscillator

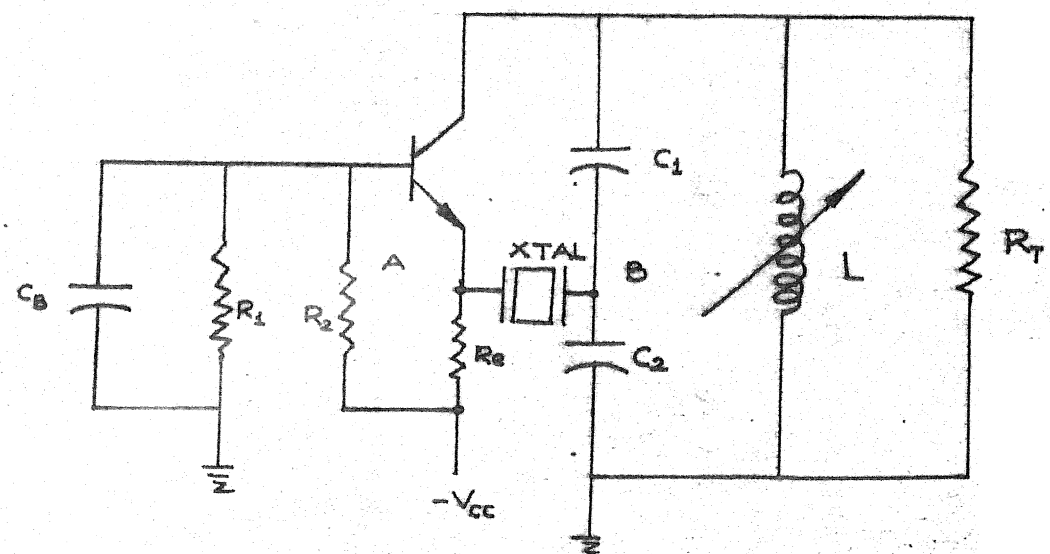
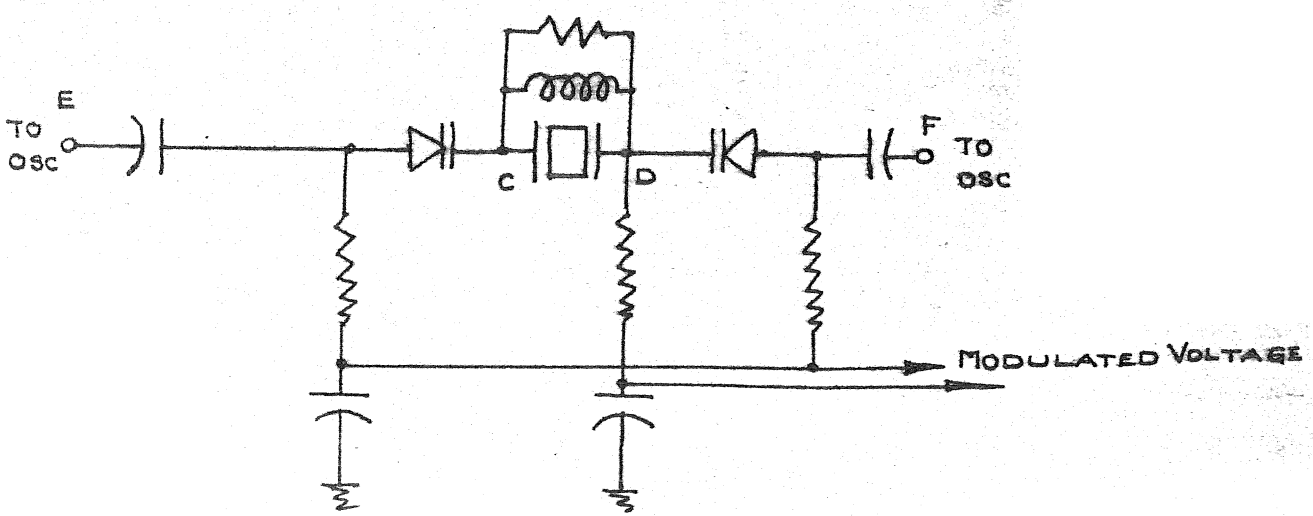


FIG. 4.11(b) VCXO Modulator Schematic



oscillations to stabilise. The step by step design procedure of this oscillator is discussed in Ref. 9, Fig. 4.11(b) is the modification of the circuit Fig. 4.11(a) between A & B to provide chirping over 60 MHz carrier frequency. By properly choosing the value of inductance (L) and varactor diode one can obtain the continuous slope in the reactance Vs w axis. This facilitates perfect locking of the phase locked loop and also provides chirping increasing in frequency or decrease in frequency.

Case (a) : If Fig. 4.11(b) is inserted in Fig. 4.11(a) between A & B we get a maximum chirp width of less than 5 KHz as the chirp width is being controlled by crystal bandwidth. Case (b): In Fig. 4.11(b) if C & D points are shorted then we can get the chirp width (Δf)up to 10 KHz. Case (c): In Fig. 4.11(b) if point E is connected to B and point F to ground in fig. 4.11(a) then we can get chirp width (Δf) up to 1 MHz. But the stability wise, the short term stability will decrease as we go from case (a) to case (c).

The block diagram of the chirp synthesizer is shown in Fig. 4.12.

Since we need better stability of the V.C.O the reference frequency should be very high to provide high loop band width, there by the stability of the VCO will be achieved to the

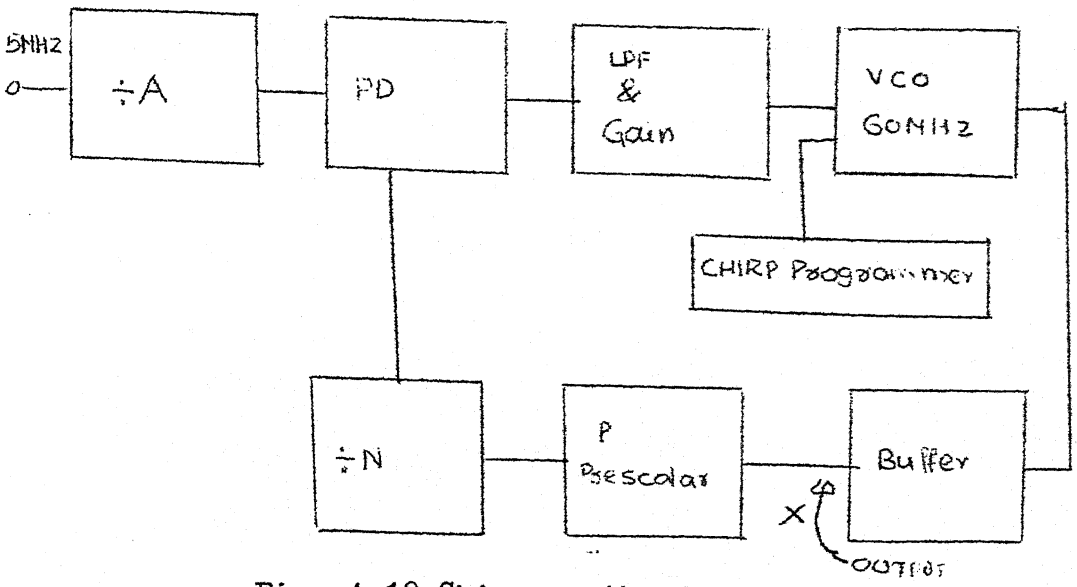


Fig. 4.12 Chirp synthesizer

degree of accuracy required. Hence the f_{ref} is chosen as 1 MHz. Now the parameters A, N, P are 5, 6 and 10 respectively.

Again for the low pass filter the second order is chosen. Also the same configuration as designed for programmable frequency synthesizer is used. Using the equations (4.10), (4.11) and (4.12), loop filter values R_1, R_2 & C can be calculated.

As before we select the w_n ten times the reference frequency; choose w_n as 10 KHz. The loop lock up time is

$$t = \frac{w_n t}{w_n} = \frac{4.5}{10 \times 10^3} = 0.45 \text{ m sec}$$

For the VCO used in case (b) 1.0 KHz chirp width K_V has found to be 5 KHz/V. If we choose R_1 = 5 K then C is given by

$$C = \frac{0.12 \times 5 \times 10^3}{60 \times (10)^2 \; 10^6 \times 5 \times 10^3} = 20 \text{ pF}$$

and $$R_2 = \frac{2\delta}{w_n C} = \frac{2 \times 0.8}{10 \times 10^3 \times 20 \times 10^{-12}} \qquad R_2 = 8 \text{ M}\Omega$$

These are the starting values for the loop filter. One has to optimise these by testing the circuit to achieve the required results.

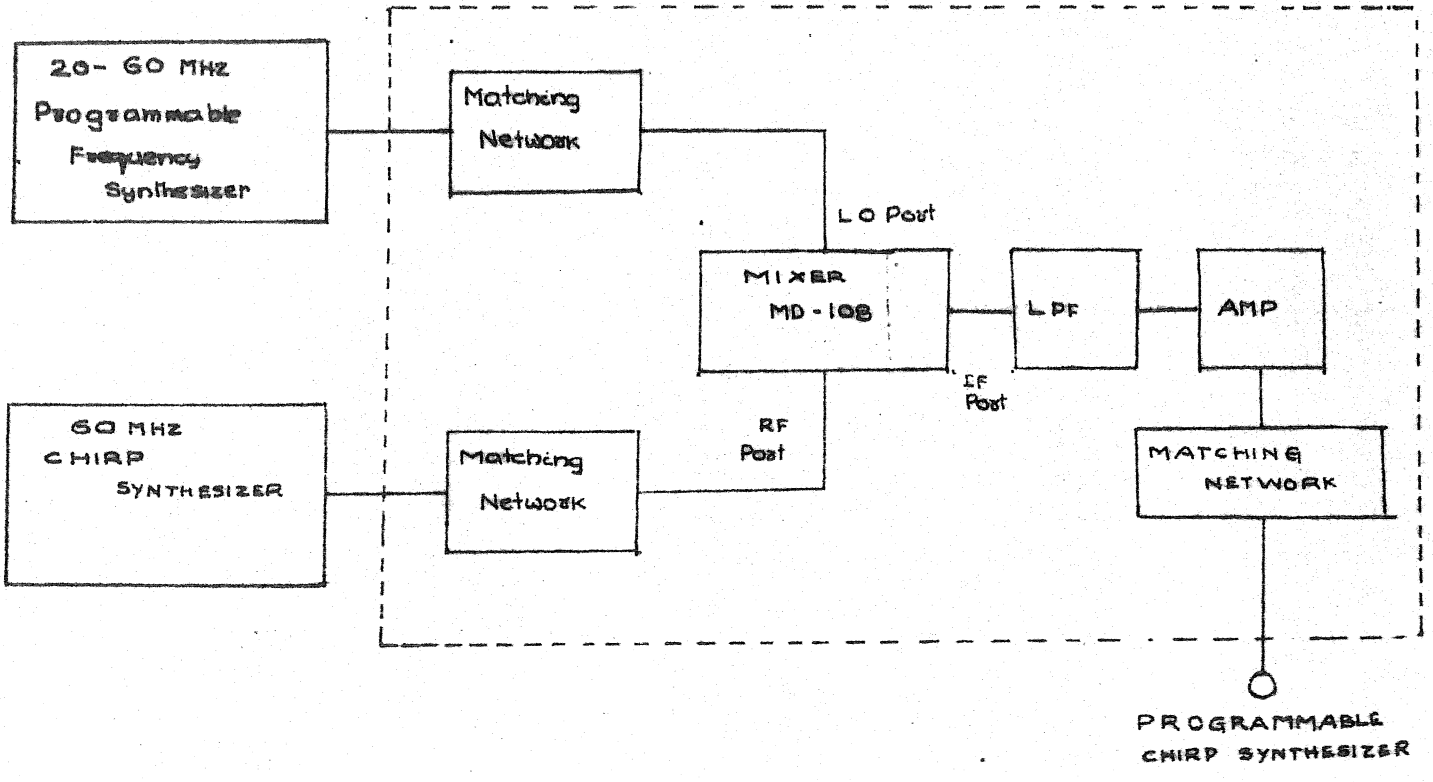
The programmable sweep generator module developed by S.M Rao towards his M.Tech thesis facilitates to control the chirp width, chirp rate and chirp repetition frequency.

4.3 Programmable Chirp Synthesizer :

The block schematic of the programmable chirp synthesizer is shown in Fig. 4.13. The operation is self explanatory from the Fig. 4.13-

ANZAC MD -108 mixer is chosen for mixing-MD-108 has an input impedance of 50Ω both at RF port and Lo port and an output impedance of 50Ω at the IF port. The output's of chirp synthesizer and programmable frequency synthesizer are buffered to give an output impedance of 220Ω. Hence matching networks are selected between mixer and programmable frequency synthesizer, and between mixer and chirp synthesizer. The design procedure for the matching network are outlined in Appendix I.

FIG 4.13 PROGRAMMABLE CHIRP SYNTHESIZER



7th order chebyshev low pass filter is designed to select the lower side band at the output of the mixer. The low pass filter input and output impedances are designed as 50Ω to match the output of the mixer and the amplifier. The design procedure of the low pass filter is given in Appendix II. Finally the amplifier is also designed to give an output amplitude of 1V peak to peak into 50Ω impedance.

The chirp carrier frequencies can be obtained by removing the chirp programmer output at the VCO control line. So to get the chirp and its carrier frequencies simultaneously one has to implement the block diagram Fig. 4.13 with and without chirp programmer.

4.4 Implementation :

The programmable chirp synthesizer is implemented in three modules using design background developed in previous sections. A little modifications have made in the final circuit to achieve the required goals. The values designed in previous sections are also optimised for better performance. The final circuit diagrams are shown in Fig. 4.14 and Fig. 4.15. The modules are designed according to CAMAC standards. Programmable frequency synthesizer is implemented in one module which has a provision for CAMAC control as well as manual

control in the front panel chirp synthesizer and programmable chirp synthesizer are implemented in the second module. The chirp reference frequency generator is implemented in the third module. These are shown in Fig. 4.16.

In the next chapter the experiments conducted and results obtained are discussed.

CHAPTER V

EXPERIMENTS AND RESULTS

The following experiments were conducted on programmable chirp synthesizer implemented in three modules and the results obtained are given.

1. Stability :

The stability of the chirp synthesizer without chirp is tested using hp frequency counter which has a stability of 1 in 10^8 and a resolution of 1 Hz.

i) Long term stability :

The system was kept on for three hours and it was found the frequency was varying not more than $\pm$ 10 Hz

ii) Short term stability :

It was observed on the counter that there is $\pm$ 10 Hz variation over 60 MHz due to the noise sitting on V.C.O control line. It can be minimized by providing a proper shielding for the V.C.O control line from other noise sources.

Stability measurements made, give only the rough orders of magnitude indications of the stabilities. No rigourous test procedures were adopted.

2. Capture range :

The capture range of PLL in case (a) of chirp synthesizer

is found to be 25-30 KHz and in case (b) it is roughly 100 KHz. It was also found that some times the PLL goes out of lock because of the supply disturbances. This problem can be eliminated by providing proper supply decoupling between module and power supply.

2. Frequency Range :

The frequency range of the programmable chirp frequency synthesizer is tested. It was found that the frequency range is limited to 500 KHz to 30 MHz. Wider range of frequencies can be obtained by using two cascaded low pass filters and a wide band amplifier.

3. The Chirp Linearity :

The chirp linearity by varying chirp rate, chirp width, chirp repetition frequency is tested by using the following set up (Fig. 5.1). The test was conducted for the chirp width of $\Delta f < 10$ KHz.

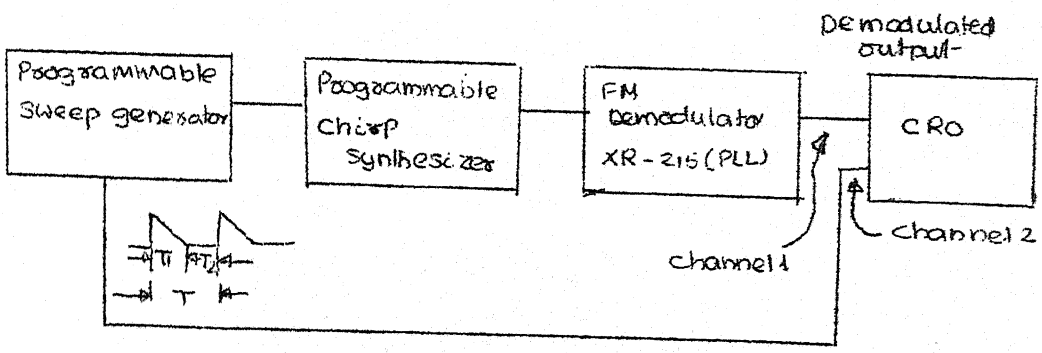


Fig. 5.1 Chirp linearity test set up

At the output of the programmable sweep generator a saw-tooth wave form is generated whose amplitude A_1, interval T_2 can be controlled. FM demodulator XR- 215 (PLL) is designed for 3.6 MHz. Hence the carrier frequency of the chirp is set to 3.6 MHz. Now by applying chirp input from programmable sweep generator, the wave forms obtained on a C.R.O under three set of conditions for A_1 and T_2 are shown in Fig. 5.2. Fig. 5.3 and 5.4. It can be seen from Fig. 5.2, Fig. 5.3 & Fig. 5.4 that the linearity of the chirp signal improves as the chirp repetition frequency decreases. This is understandable because as the chirp repetition frequency decreases sufficient time is available for the loop to settle down to rest state. The above statement is verified by making T_2, the chirp interval is zero. It can be seen from Fig. 5.4, the demodulated ramp is non linear and also the PLL does not respond to the ramp input during some intervals of time.

4. Chirp Spectrum :

The following test set up (Fig. 5.5) was used to find the chirp spectrum of the chirp synthesizer for different values of time band width products ($T^{\$}\Delta f$).

It is found from the chirp linearity test, when the ramp interval $T_2 = 0$, the demodulated output is nonlinear and also PLL does not respond to some intervals of the ramp input.

This problem in chirping is eliminated by applying a triangular wave which has zero d.c value. It was found that the chirp linearity will be improved and uniform for wider frequency range of traiangle input as long as the loop time const is for greater than the period T of the traiangle waveform. The demodulated output of XR - 215 and input traiangle wave observed on a C.R.O for one set of chirp width and time period T is shown in Fig. 5.6. It was also found that if T is equal to the loop time constant, the loop tracks the input variations on the VCO control line in the negative direction and hence the loop is always locked to 60 MHz.

Using the traiangle wave form as input at the VCO control line the chirp spectrum was observed using the test set up Fig. 5.5, for five sets of chirp width (Δf) and chirp sweep time. The wave forms observed on spectrum analyzer are shown in Fig. 5.7(a) to (e). It is observed from the fig. 5.6(a) to (e) that the chirp spectrum becomes more and more flat as the time band width product $T^{*}\Delta f$ increases as it was stated in the chirp spectrum analysis section 2.2 case (b) and showed in Fig. 2.2.

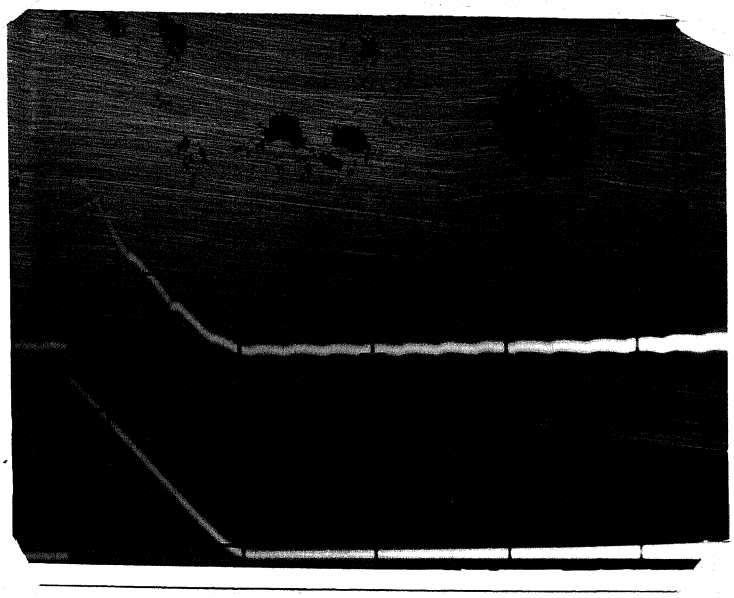


Fig. 5.2 Chirp linearity upper trace demodulated output, lower trace input ramp.

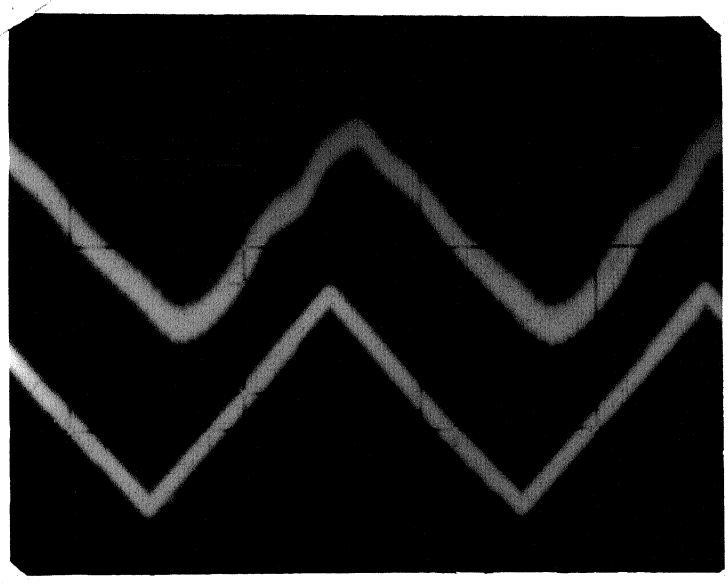


Fig. 5.6 Chirp linearity for a triangle wave input f = 12.5KHz, chirp-repetition frequency 900 Hz

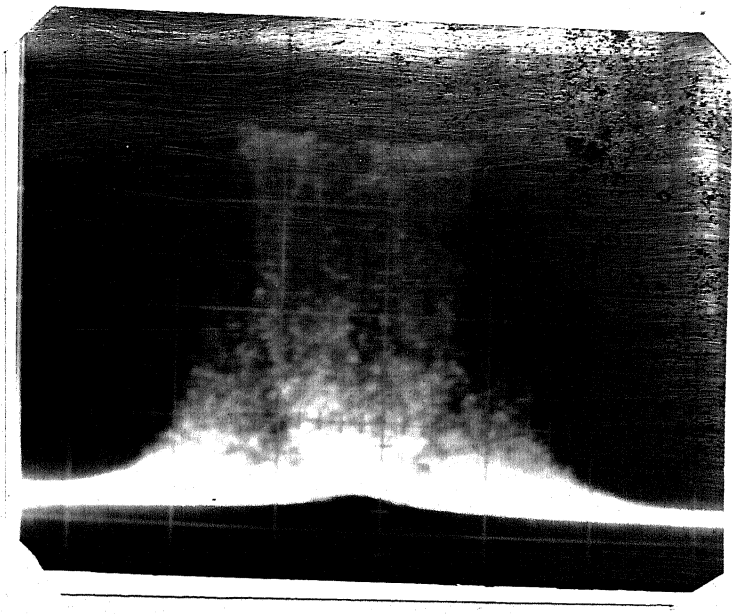


Fig. 5.7(a) f = 12.5 KHz, Chirp repetition frequency 90 Hz, $T\Delta f$ = 140

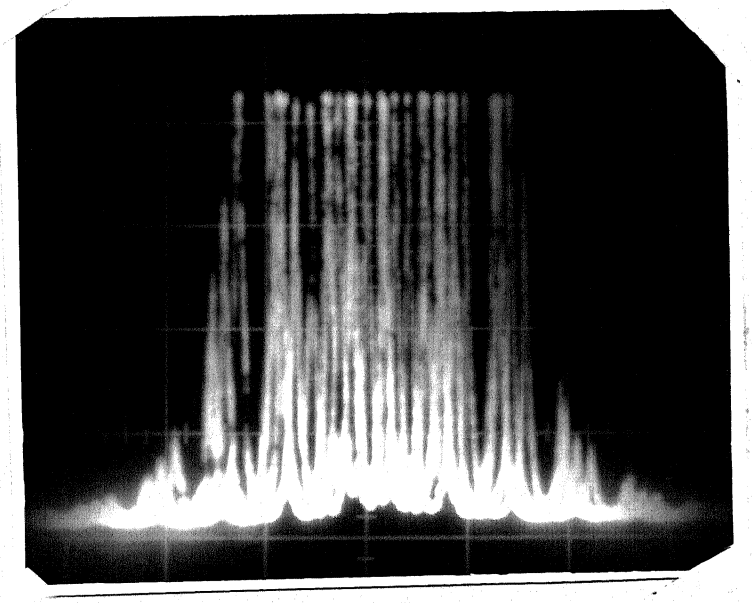


Fig. 5.7(b) f = 12.5 KHz, Chirp repetition frequency 900 Hz, $T\Delta f$ = 14

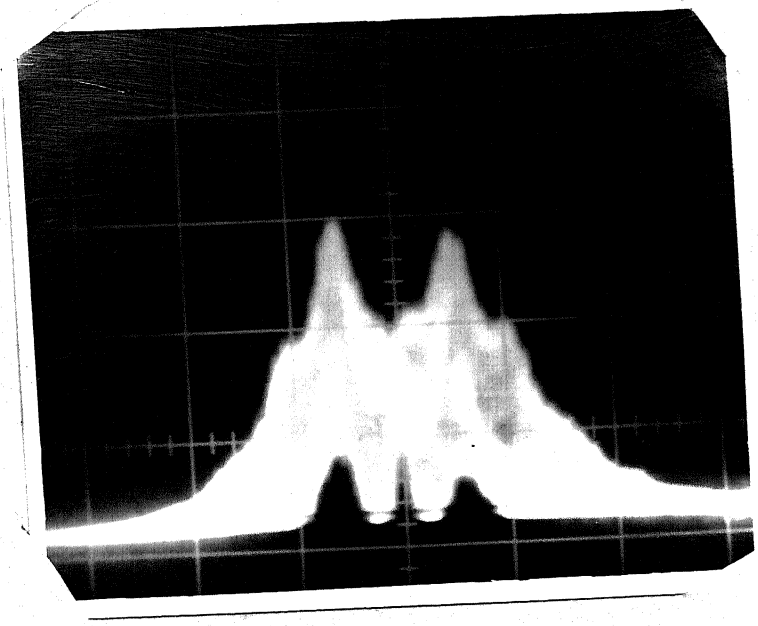


Fig. 5.7(c) Chirp width 12.5 KHz, chirp repetition frequency 3KHz, $T\triangle f=4$

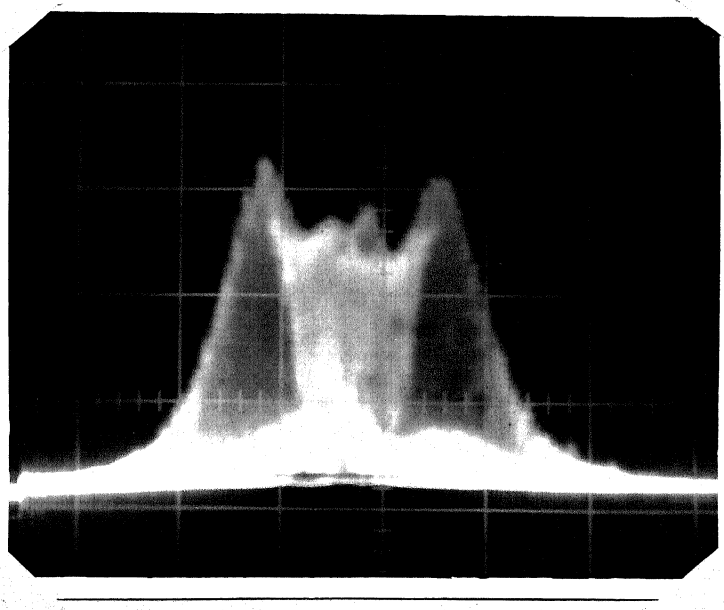


Fig. 5.7(d) Chirp width 15 KHz, chirp repetition frequency 300 Hz, $T\triangle f = 50$

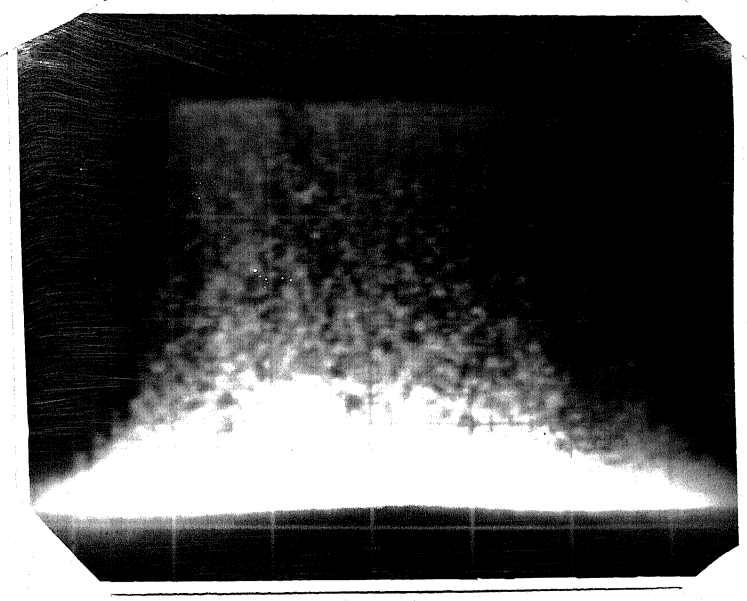


Fig. 5.7(e) Chirp width = 20 KHz chirp repetition frequency: 3Hz; T△ f: 6000

CHAPTER VI

CONCLUSIONS

The RF programmable chirp synthesizer is designed and implemented in three modules. It was tested and found to be capable of providing a wide range of frequencies from 500 KHz - 30 MHz. It has a provision to provide carrier frequency of the chirp simultaneously. It is found that the maximum chirp width is 10 KHz. And it was also found the chirp is linear only under certain conditions. Also it was found that there should be some finite amount of time between two successive chirps for the loop to settle to the rest state in case of ramp input at the VCO control line. The time rate of chirp (α) is also being limited by the characteristics of varactor diode.

The following scheme (Fig. 6.1) is suggested to overcome some of the above problems.

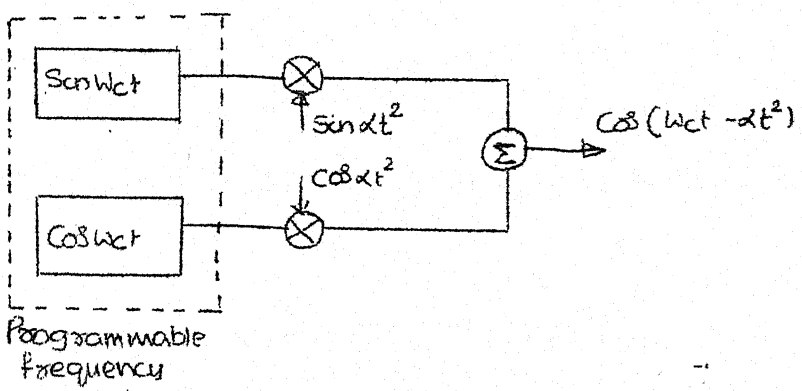


Fig. 6.1 QAM chirp generation

Chirp transfer function analyzer is developed keeping in mind its possible use in NMR spectrometer. This system need be tested, for its feasibility as an addon to a CW NMR spectrometer.

APPENDIX I

MATCHING NETWORKS : [Ref.10]

The suggested matching network for $R_1 > R_L$ is shown in Fig. A.1. The design equations are as follows.

First select the required Q, then C_1 , C_2 and L can be obtained from the following equations.

$$X_{C1} = R_1/Q \qquad (A.1)$$

$$X_{C2} = R_L \sqrt{\frac{R_1/R_L}{(Q^2+1)-R_1/R_L}} \qquad (A.2)$$

$$X_L = \frac{Q\,R_1+(R_1\,R_L/X_{C2})}{Q^2+1} \qquad (A.3)$$

For example the VCXO matching network can be designed as :

Select Q = 20 ; then $X_{C1} = \frac{220}{20} = 11$

For R_1 = 220 Ω; and R_L = 50 Ω

$$X_{C2} = 50\sqrt{\frac{220/50}{(400+1)-\frac{220}{50}}} = 12$$

$$X_L = \frac{20\text{x}220 + (220\text{x}50/12)}{401} = 13.25$$

Hence, C_1, C_2, L can be obtained for f = 60 MHz as 220 pF, 220 pF and L = 500 nH respectively.

APPENDIX II

CHEBYSHEV LOW PASS FILTER

The design and analysis of Chebyshev low pass filters is carried in Ref. 11 . Using the design equations the 7th order low pass filter is designed below.

Normalized frequency $= \sim = f/f_r$

Normalized resistance $= \vee = R/R_r$

Normalized inductance $= L' = \frac{w_r L^r}{R_r}$

Normalized capacitance $= C' = w_r C R_r$

The normalized values for a 7th order filter shown in Fig. A-2, when $R_S = R_L$ are given as:

$L_1' = 1.2615$ $\quad C_2' = 1.5196$

$L_3' = 2.2392$ $\quad C_4' = 1.6804$

$L_5' = 2.2392$ $\quad C_6' = 1.5196$

$L_7' = 1.2615$

The reference values can be obtained as:

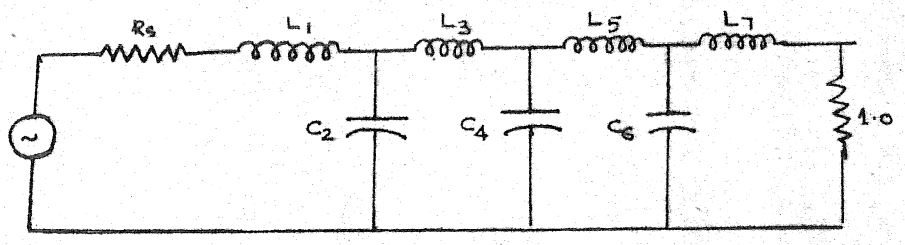
$$L_r = \frac{R_L}{w_c}$$ where R_L = load impedance and w_c = cut off frequency

$$C_r = \frac{1}{R_L w_c}$$

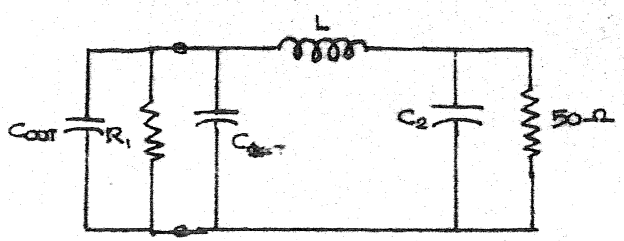
The actual values can be obtained from:

$L_x = L_r$ x normalized value

$C_x = C_r$ x normalized value



A-2 7th Order Chebyshev LPF



A-1 Matching Network

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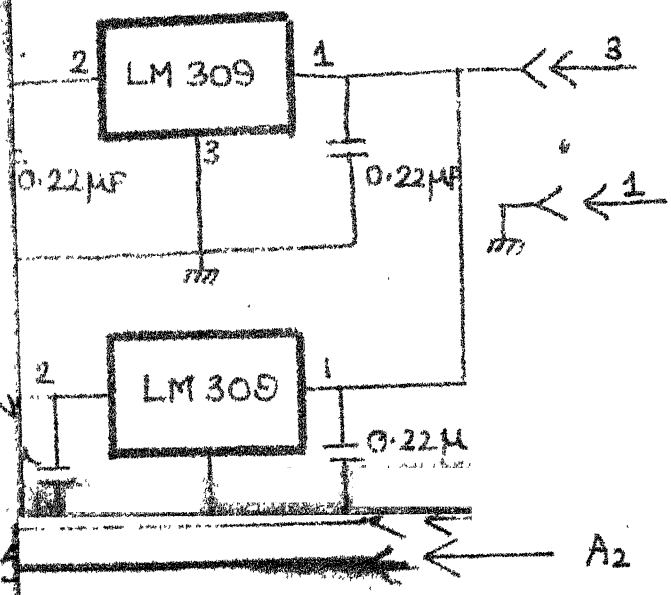
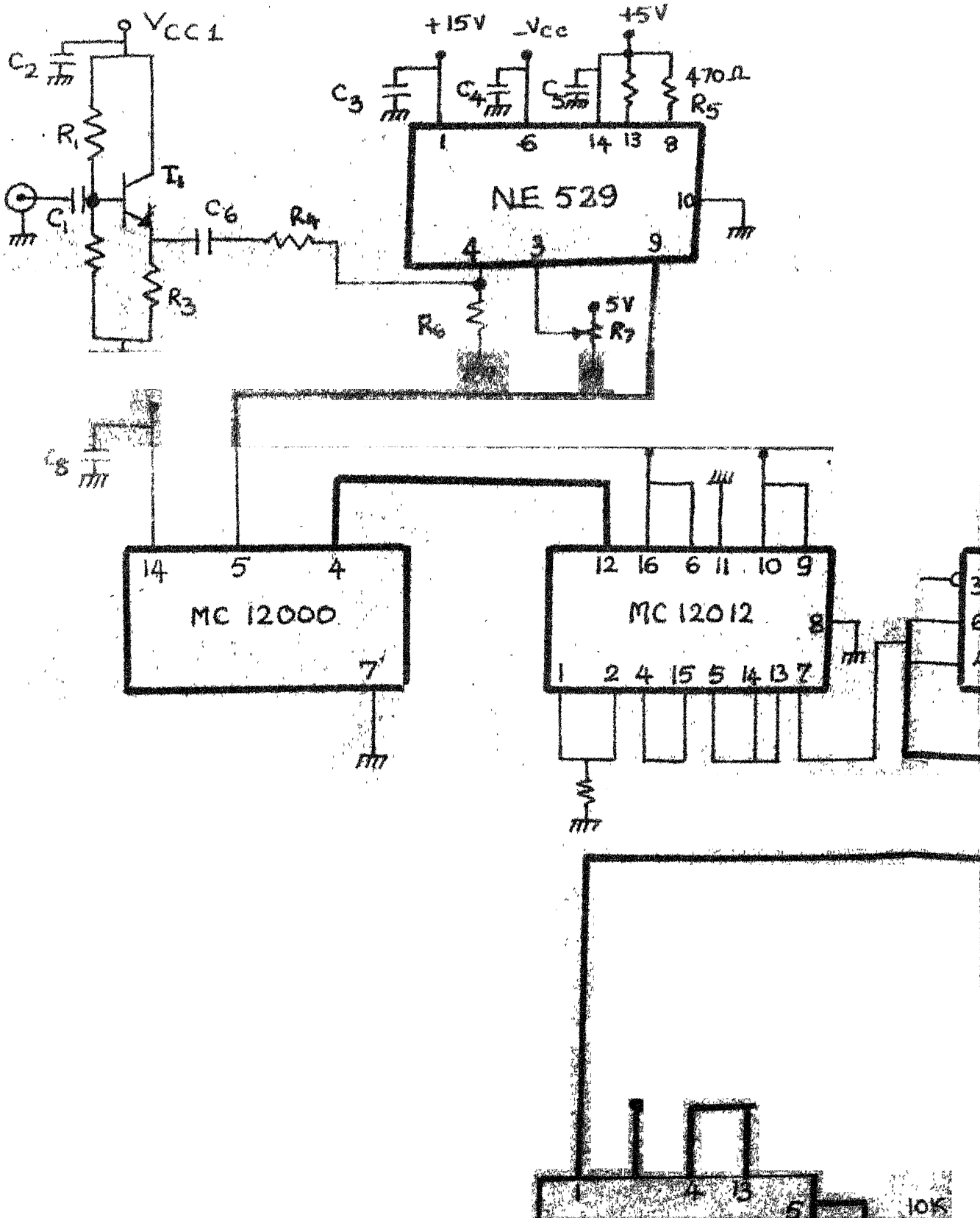


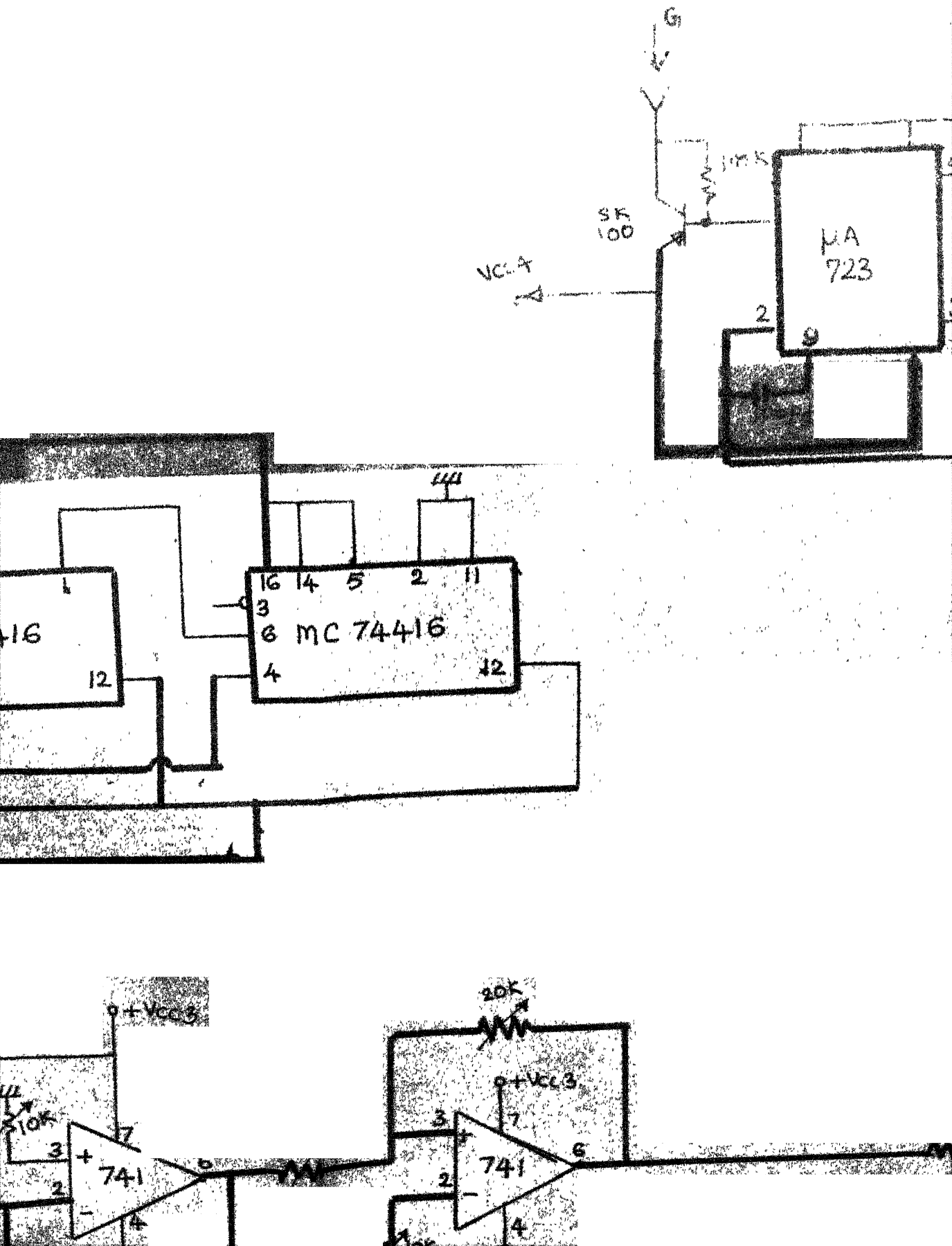
FREQUENCY SYNTHESIZER

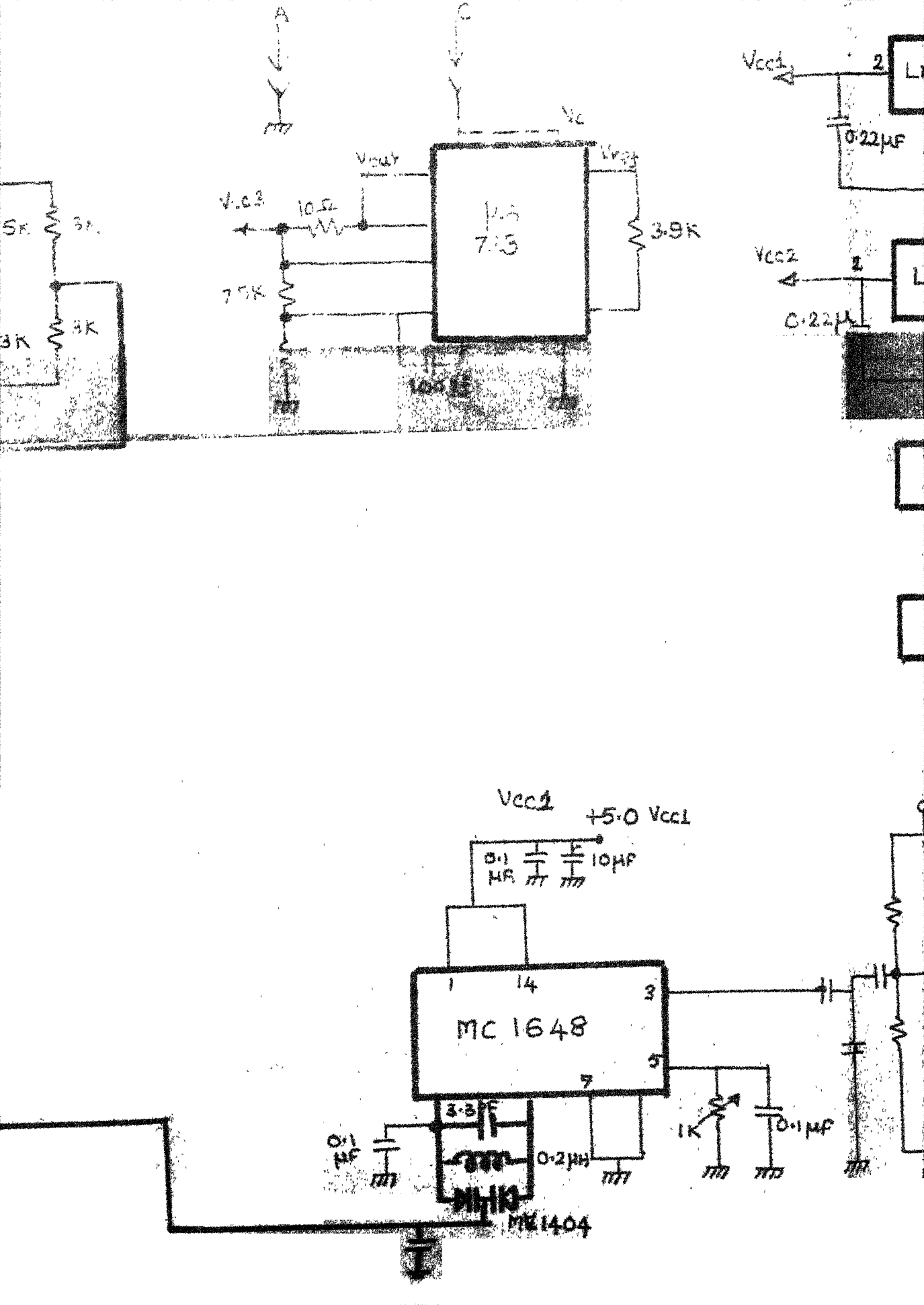
UIT SCHEMATIC

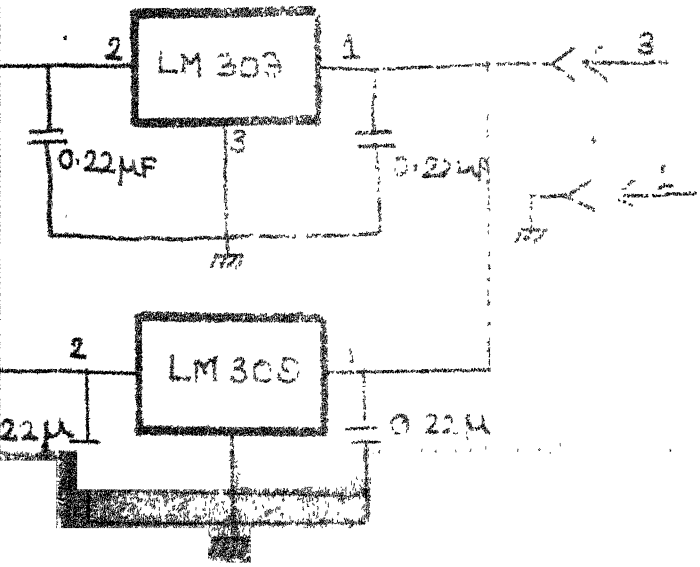
BY: B. P. CHOWDARY.

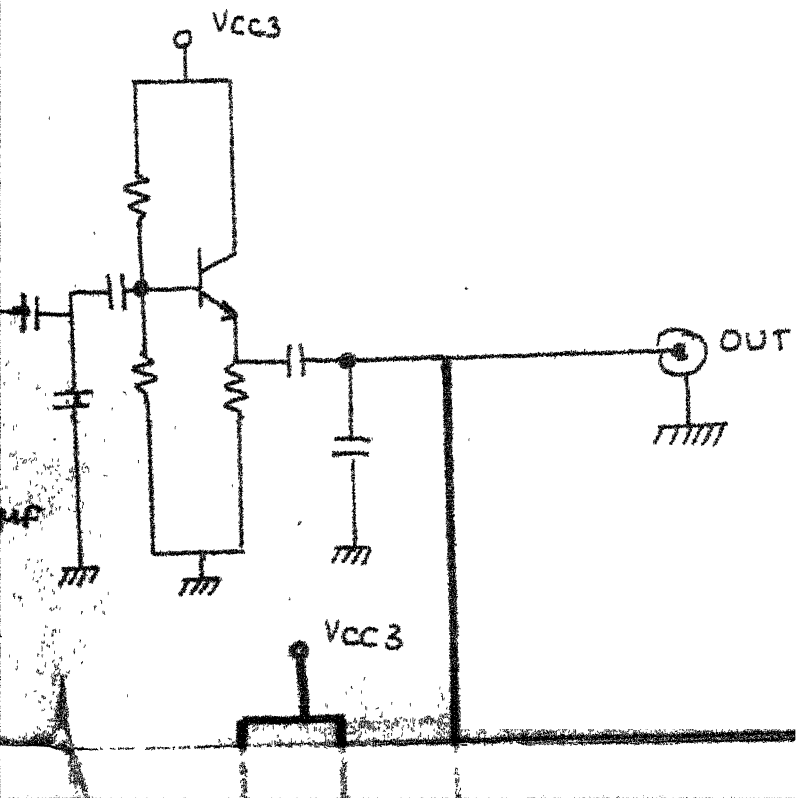
BY : G. N. M. SUDHAKAR

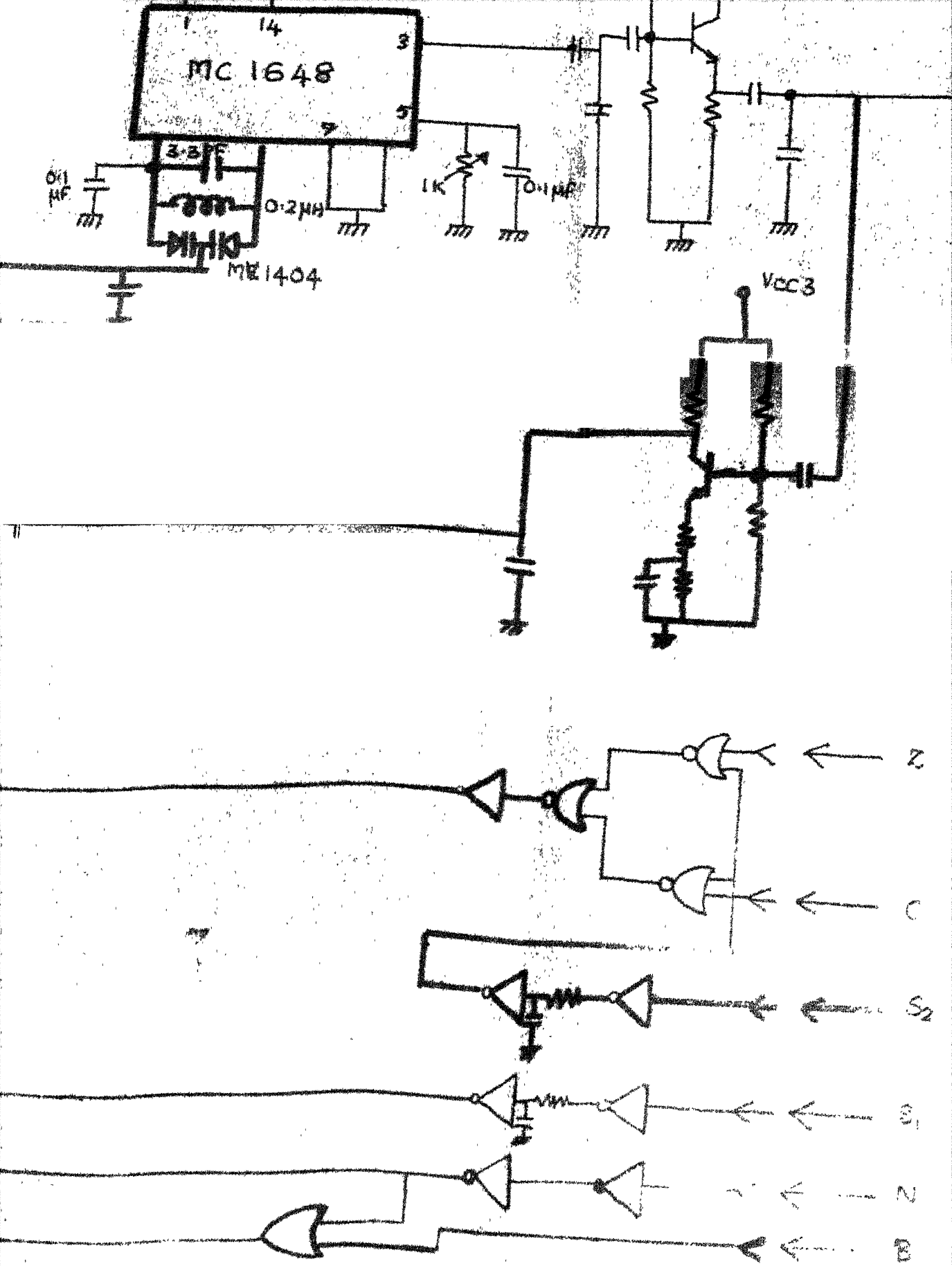

V_{CC1}
C_2
R_1
T_1
C_1
C_6
R_4
R_3
+15V
$-V_{cc}$
+5V
C_3
C_4
C_5
470Ω
R_5
1
6
14
13
8
NE 529
10
4
3
9
R_6
5V
R_7
C_8
14
5
4
MC 12000
7
12
16
6
11
10
9
MC 12012
8
1
2
4
15
5
14
13
7
1
4
13
6
10K

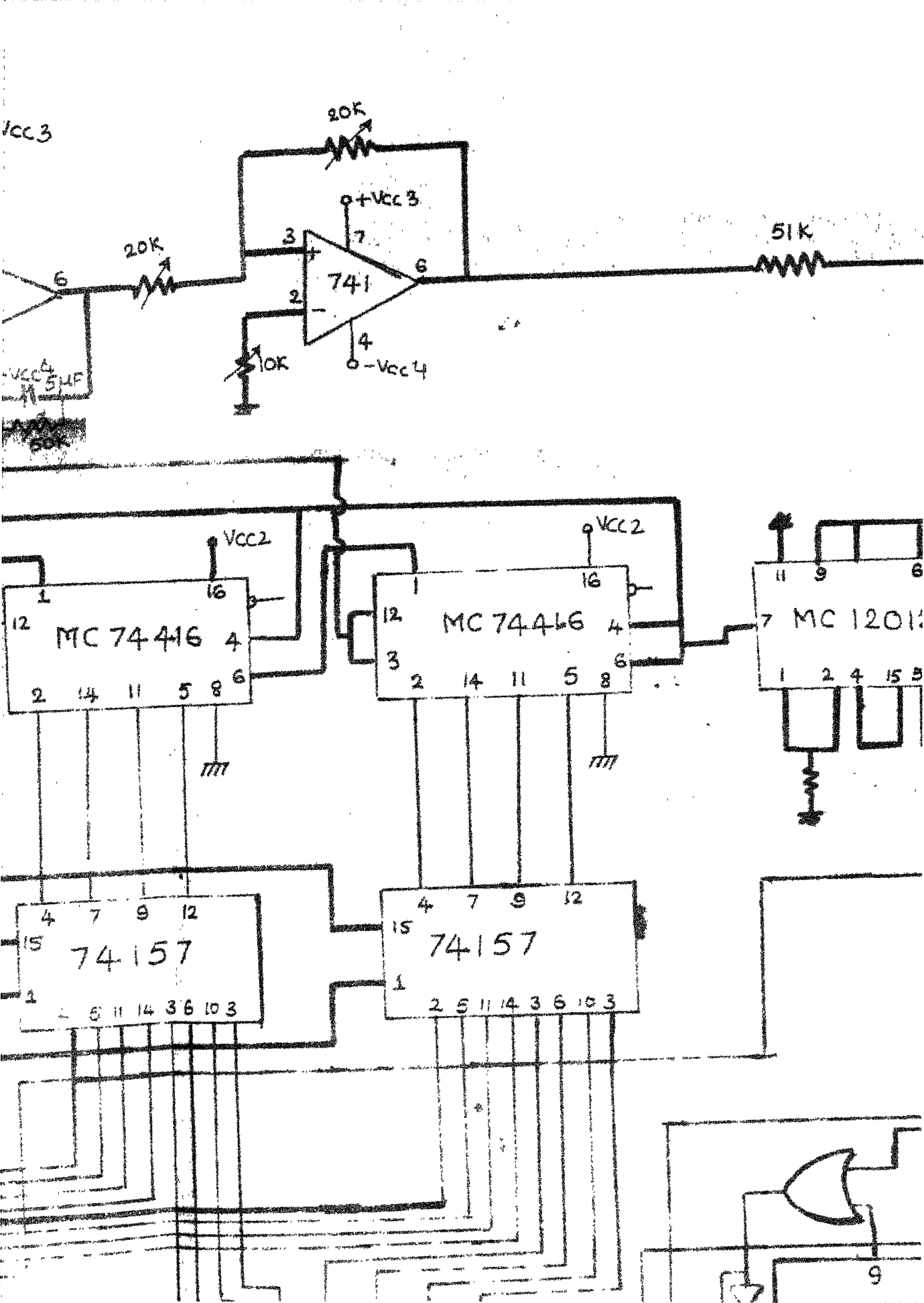

G
SK
100
VCC
μA
723
2
9
16
14
5
2
11
3
6
MC 74416
4
12
741
741
20K
+Vcc
+Vcc

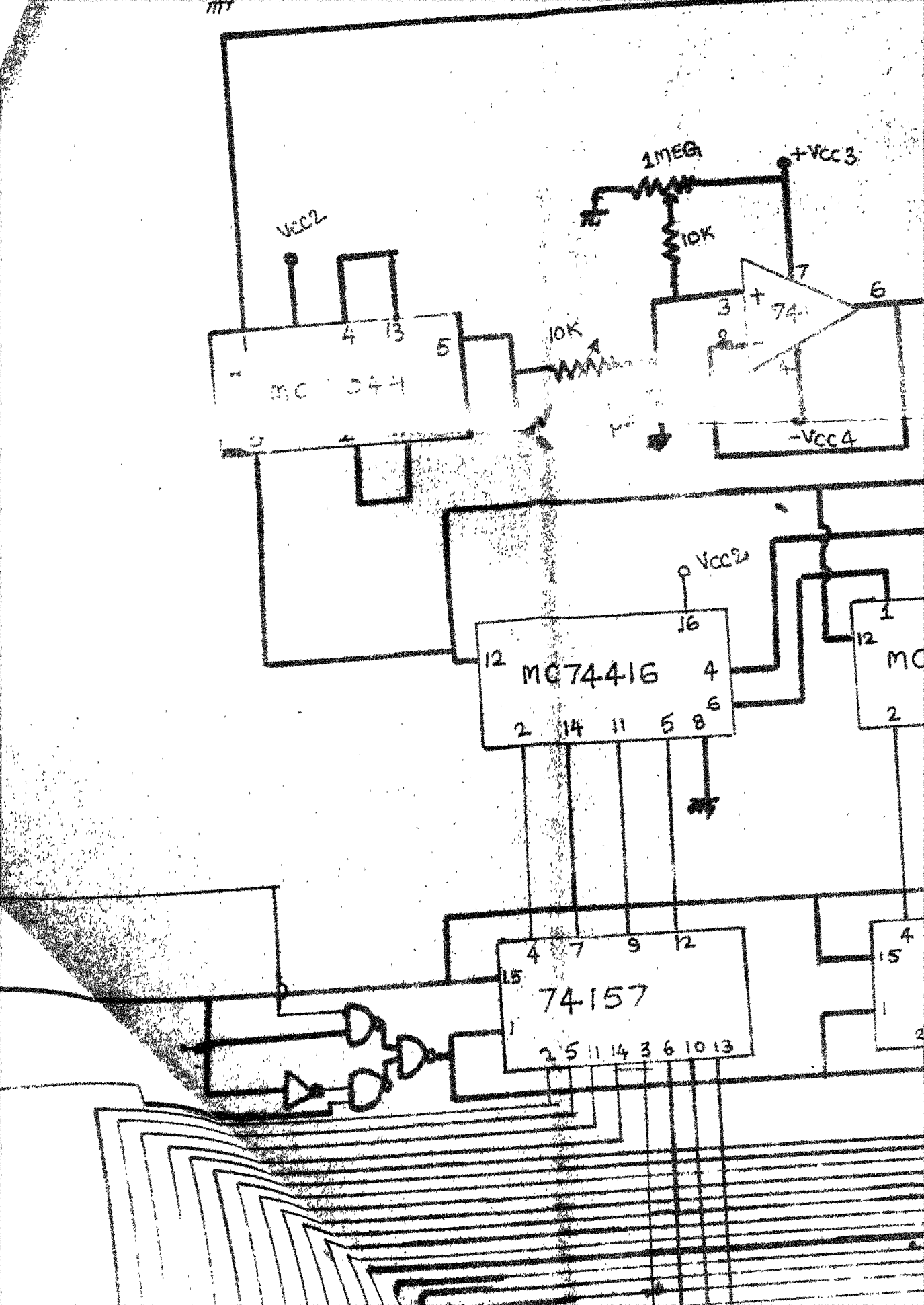

A
C
Vc
Vcc3
10.5Ω
7.5K
3.9K
MC 1648
Vcc1
0.22μF
Vcc2
0.22μ
5K
3K
3K
3K
Vcc1
+5.0 Vcc1
0.1 μF
10μF
1
14
3
5
7
MC 1648
3.3
0.1 μF
0.2μH
1K
0.1μF
MC1404

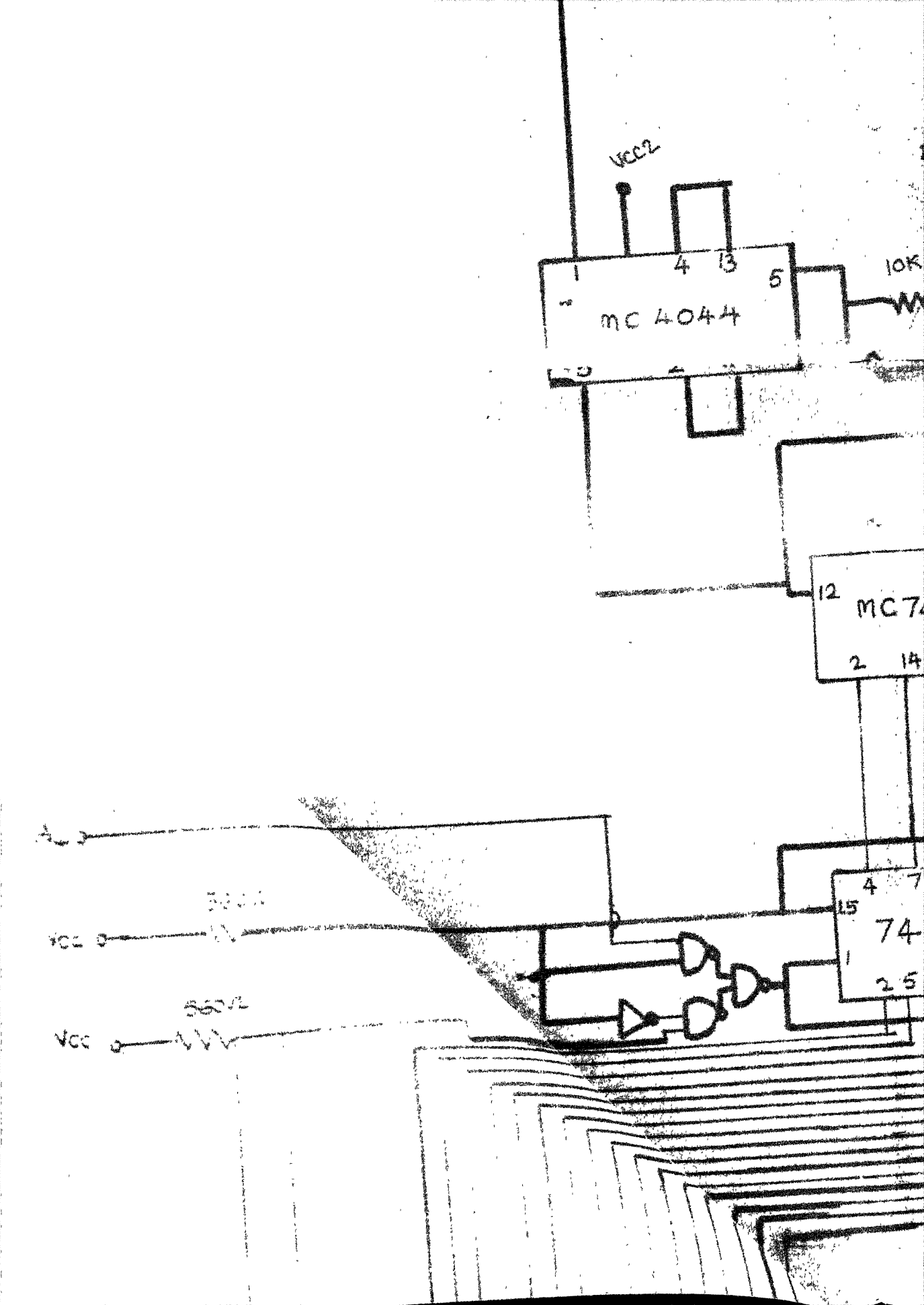

2
LM 309
1
3
0.22μF
3
0.22μF
2
LM 309
0.22μ
0.22μ


Vcc3
OUT
Vcc3


1
14
MC 1648
3
5
7
3.3 pF
0.1 μF
0.2 μH
1K
0.1 μF
MC1404
Vcc3
Z
C
S2
S1
N
B


Vcc3
20K
+Vcc3
3
7
741
6
2
4
-Vcc4
10K
20K
6
51K
Vcc2
MC 74416
MC 74446
MC 1201
74157
74157
9


1MEG
+Vcc3
10K
Vcc2
7
6
3
2
4
74
1
4
13
5
MC
10K
-Vcc4
Vcc2
16
12
MC74416
4
6
2
14
11
5
8
1
12
MC
2
4
7
9
12
15
74157
1
2
5
11
14
3
6
10
13
4
15
1
2


VCC2
1
4
13
5
MC 4044
10K
12
MC 7
2
14
4
7
15
74
1
2
5
VCC
VCC